(19)日本国特許庁（ＪＰ）　(12)公開特許公報（A）　(11)特許出願公開番号
特開2001－267242
（P2001－267242A）
(43)公開日　平成13年９月28日(2001.9.28)

(51)Int.Cl.⁷	識別記号	FI	テーマコード（参考）
H01L 21/205		H01L 21/205	5F041
33/00		33/00	C 5F045
H01S 5/343		H01S 5/343	5F073

審査請求　未請求　請求項の数13　ＯＬ　（全 18 頁）

(21)出願番号　特願2000－71350(P2000－71350)

(22)出願日　平成12年３月14日(2000.3.14)

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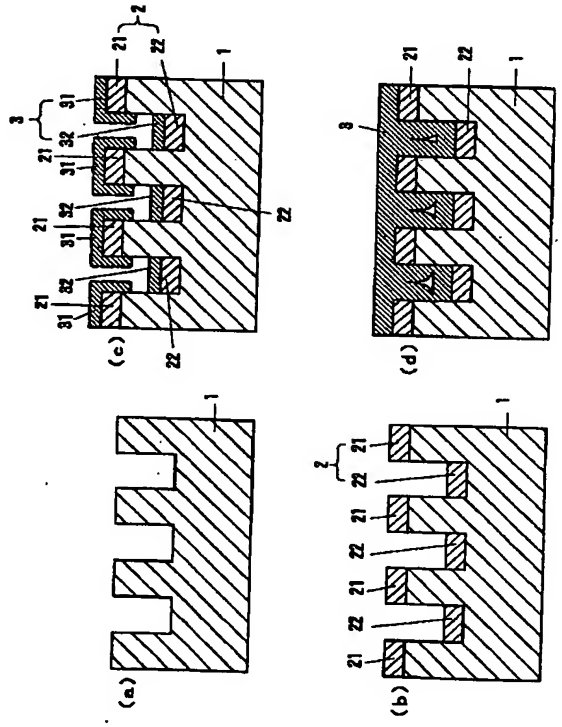
(54)【発明の名称】　ＩＩＩ族窒化物系化合物半導体及びその製造方法

(57)【要約】
【課題】貫通転位の少ない領域を有するIII族窒化物系化合物半導体を提供すること。
【解決手段】サファイア基板１を幅10μm、間隔10μm、深さ10μmのストライプ状にエッチングする。次にAlNのバッファ層２を約40nmの厚さに基板１の段差の主に上段面と底面に形成する。次に、縦及び横方向エピタキシャル成長によりGaN層３を形成する。この時、主に段差の上段面に形成されたバッファ層２１からの横方向エピタキシャル成長により段差が覆われ、表面が平坦となる。GaN層３の、基板１の深さ10μmの段差の底面上方に形成された部分は、段差の上段面上方に形成された部分に比して貫通転位が著しく抑えられる。



【特許請求の範囲】

【請求項１】　基板上にIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、

前記基板表面の少なくとも一部を削り、前記基板面に段差を設ける工程と、

前記基板の、削られなかった表面に点状、ストライプ状又は格子状等の島状態に形成された上面を核として、所望のIII族窒化物系化合物半導体を、前記基板の段差の下段上方をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とするIII族窒化物系化合物半導体の製造方法。

【請求項２】　基板上にバッファ層を介してIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、

前記基板表面の少なくとも一部を削り、前記基板面に段差を設ける工程と、

前記バッファ層を前記基板に形成する工程と、

前記基板の、削られなかった表面に点状、ストライプ状又は格子状等の島状態に形成された前記バッファ層を核として、所望のIII族窒化物系化合物半導体を、前記基板の段差の下段上方をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とするIII族窒化物系化合物半導体の製造方法。

【請求項３】　基板上にバッファ層を介してIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、

前記基板表面の少なくとも一部を削り、前記基板面に段差を設ける工程と、

前記バッファ層を前記基板に形成する工程と、

前記バッファ層上にIII族窒化物系化合物半導体を縦方向エピタキシャル成長させて単結晶層を形成する工程と、

前記基板の、削られなかった表面に点状、ストライプ状又は格子状等の島状態に形成された前記バッファ層上の前記III族窒化物系化合物半導体の単結晶層を核として、所望のIII族窒化物系化合物半導体を、前記基板の段差の下段上方をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とするIII族窒化物系化合物半導体の製造方法。

【請求項４】　基板上にバッファ層を介してIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、

前記バッファ層を前記基板に形成する工程と、

前記バッファ層と前記基板表面の少なくとも一部を削り、前記基板面に前記バッファ層の形成された上段と、前記バッファ層の形成されていない下段との段差を設ける工程と、

前記基板の、削られなかった表面に点状、ストライプ状又は格子状等の島状態に形成された前記バッファ層を核として、所望のIII族窒化物系化合物半導体を、前記基板の段差の下段上方をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とするIII族窒化物系化合物半導体の製造方法。

【請求項５】　基板上にバッファ層を介してIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、

前記バッファ層を前記基板に形成する工程と、

前記バッファ層上にIII族窒化物系化合物半導体を縦方向エピタキシャル成長させて単結晶層を形成する工程と、

前記III族窒化物系化合物半導体の単結晶層と前記バッファ層と前記基板表面の少なくとも一部を削り、前記基板面に前記III族窒化物系化合物半導体の単結晶層と前記バッファ層の形成された上段と、前記III族窒化物系化合物半導体の単結晶層及び前記バッファ層の形成されていない下段との段差を設ける工程と、

前記基板の、削られなかった表面に点状、ストライプ状又は格子状等の島状態に形成された前記バッファ層上の前記III族窒化物系化合物半導体の単結晶層を核として、所望のIII族窒化物系化合物半導体を、前記基板の段差の下段上方をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とするIII族窒化物系化合物半導体の製造方法。

【請求項６】　基板上にIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、

前記基板表面の少なくとも一部の平滑度を悪化させ、前記III族窒化物系化合物半導体層が充分には形成されない部分を前記基板表面に形成する表面処理工程と、

前記III族窒化物系化合物半導体を前記基板に形成し、前記III族窒化物系化合物半導体の単結晶層が充分に形成された部分と、前記III族窒化物系化合物半導体の単結晶層が充分には形成されていない部分とを形成する工程と、

前記基板の平滑度を悪化させていない部分に、点状、ストライプ状又は格子状等の島状態に形成された前記III族窒化物系化合物半導体の単結晶層を核として、前記III族窒化物系化合物半導体を、前記III族窒化物系化合物半導体の単結晶層が充分には形成されていない部分をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とするIII族窒化物系化合物半導体の製造方法。

【請求項７】　基板上にバッファ層を介してIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、

前記基板表面の少なくとも一部の平滑度を悪化させ、前記バッファ層が充分には形成されない部分を前記基板表面に形成する表面処理工程と、

前記バッファ層を前記基板に形成し、前記バッファ層が

充分に形成された部分と、前記バッファ層が充分には形成されていない部分とを形成する工程と、
前記基板の平滑度を悪化させていない部分に、点状、ストライプ状又は格子状等の島状態に形成された前記バッファ層を核として、所望のIII族窒化物系化合物半導体を、前記バッファ層が充分には形成されていない部分をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とするIII族窒化物系化合物半導体の製造方法。
【請求項８】　基板上にバッファ層を介してIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、
前記基板表面の少なくとも一部の平滑度を悪化させ、前記バッファ層が充分には形成されない部分を前記基板表面に形成する表面処理工程と、
前記バッファ層を前記基板に形成し、前記バッファ層が充分に形成された部分と、前記バッファ層が充分には形成されていない部分とを形成する工程と、
前記バッファ層が充分に形成された部分にIII族窒化物系化合物半導体の単結晶層を形成する工程と、
前記基板の平滑度を悪化させていない部分に形成された、点状、ストライプ状又は格子状等の島状態の前記バッファ層上の前記III族窒化物系化合物半導体の単結晶層を核として、所望のIII族窒化物系化合物半導体を、前記バッファ層が充分には形成されていない部分をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とするIII族窒化物系化合物半導体の製造方法。
【請求項９】　基板上にバッファ層を介してIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、
前記バッファ層を前記基板に形成する工程と、
前記バッファ層表面の少なくとも一部の平滑度を悪化させ、III族窒化物系化合物半導体の単結晶層が充分には形成されない部分を形成する表面処理工程と、
前記平滑度を悪化させていない部分の、点状、ストライプ状又は格子状等の島状態の前記バッファ層を核として、所望のIII族窒化物系化合物半導体を、前記バッファ層の平滑度を悪化させた部分をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とするIII族窒化物系化合物半導体の製造方法。
【請求項１０】　基板上にバッファ層を介してIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、
前記バッファ層を前記基板に形成する工程と、
第１のIII族窒化物系化合物半導体を前記バッファ層上に形成する工程と、
前記第１のIII族窒化物系化合物半導体表面の少なくとも一部の平滑度を悪化させ、第２のIII族窒化物系化合物半導体の単結晶層が充分には形成されない部分を形成する表面処理工程と、
前記平滑度の悪化していない部分の、点状、ストライプ状又は格子状等の島状態の前記第１のIII族窒化物系化合物半導体を核として、前記第２のIII族窒化物系化合物半導体を、前記バッファ層の平滑度を悪化させた部分をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とするIII族窒化物系化合物半導体の製造方法。
【請求項１１】　請求項１乃至請求項１０のいずれか１項に記載のIII族窒化物系化合物半導体の製造方法により製造した前記III族窒化物系化合物半導体層の、横方向エピタキシャル成長した部分の上層に形成されたことを特徴とするIII族窒化物系化合物半導体素子。
【請求項１２】　請求項１乃至請求項１０のいずれか１項に記載のIII族窒化物系化合物半導体の製造方法により製造した前記III族窒化物系化合物半導体層の、横方向エピタキシャル成長した部分の上層に、異なるIII族窒化物系化合物半導体層を積層することにより得られることを特徴とするIII族窒化物系化合物半導体発光素子。
【請求項１３】　請求項１乃至請求項１０のいずれか１項に記載のIII族窒化物系化合物半導体の製造方法に加えて、横方向エピタキシャル成長した部分の上層以外を略全部除去することにより、前記III族窒化物系化合物半導体基板を得ることを特徴とするIII族窒化物系化合物半導体基板の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、III族窒化物系化合物半導体の製造方法に関する。特に、横方向エピタキシャル成長（ＥＬＯ）成長を用いる、III族窒化物系化合物半導体の製造方法並びにIII族窒化物系化合物半導体素子及びIII族窒化物系化合物半導体基板に関する。尚、III族窒化物系化合物半導体とは、例えばAlN、GaN、InNのような２元系、$Al_xGa_{1-x}N$、$Al_xIn_{1-x}N$、$Ga_xIn_{1-x}N$（いずれも$0<x<1$）のような３元系、$Al_xGa_yIn_{1-x-y}N$（$0<x<1$，$0<y<1$，$0<x+y<1$）の４元系を包括した一般式$Al_xGa_yIn_{1-x-y}N$（$0\leqq x\leqq 1$，$0\leqq y\leqq 1$，$0\leqq x+y\leqq 1$）で表されるものがある。なお、本明細書においては、特に断らない限り、単にIII族窒化物系化合物半導体と言う場合は、伝導型をｐ型あるいはｎ型にするための不純物がドープされたIII族窒化物系化合物半導体をも含んだ表現とする。
【０００２】
【従来の技術】III族窒化物系化合物半導体は、例えば発光素子とした場合、発光スペクトルが紫外から赤色の広範囲に渡る直接遷移型の半導体であり、発光ダイオード(LED)やレーザダイオード(LD)等の発光素子に応用されている。また、そのバンドギャップが広いため、他の半導体を用いた素子よりも高温において安定した動作を

期待できることから、ＦＥＴ等トランジスタへの応用も盛んに開発されている。また、ヒ素(As)を主成分としていないことで、環境面からも様々な半導体素子一般への開発が期待されている。このIII族窒化物系化合物半導体では、通常、サファイアを基板として用い、その上に形成している。

【０００３】

【発明が解決しようとする課題】しかしながら、サファイア基板上にIII族窒化物系化合物半導体を形成すると、サファイアとIII族窒化物系化合物半導体との格子定数のミスフィットにより転位が発生し、このため素子特性が良くないという問題がある。このミスフィットによる転位は半導体層を縦方向（基板面に垂直方向）に貫通する貫通転位であり、III族窒化物系化合物半導体中に$10^9 cm^{-2}$程度の転位が伝搬してしまうという問題がある。これは組成の異なるIII族窒化物系化合物半導体各層を最上層まで伝搬する。これにより例えば発光素子の場合、ＬＤの閾値電流、ＬＤ及びＬＥＤの素子寿命などの素子特性が良くならないという問題があった。また、他の半導体素子としても、欠陥により電子が散乱することから、移動度（モビリティ）の低い半導体素子となるにとどまっていた。これらは、他の基板を用いる場合も同様であった。

【０００４】これについて、図１８の模式図で説明する。図１８は、基板９１と、その上に形成されたバッファ層９２と、更にその上に形成されたIII族窒化物系化合物半導体層９３を示したものである。基板９１としてはサファイアなど、バッファ層９２としては窒化アルミニウム(AlN)などが従来用いられている。窒化アルミニウム(AlN)のバッファ層９２は、サファイア基板９１とIII族窒化物系化合物半導体層９３とのミスフィットを緩和させる目的で設けられているものであるが、それでも転位の発生を０とすることはできない。この転位発生点９００から、縦方向（基板面に垂直方向）に貫通転位９０１が伝播し、それはバッファ層９２、III族窒化物系化合物半導体層９３をも貫いていく。こうして、III族窒化物系化合物半導体層９３の上層に、所望の様々なIII族窒化物系化合物半導体を積層して半導体素子を形成しようとすると、III族窒化物系化合物半導体層９３の表面に達した転位９０２から、半導体素子を貫通転位が更に縦方向に伝搬していくこととなる。このように、従来の技術では、III族窒化物系化合物半導体層を形成する際、転位の伝搬を阻止できないという問題があった。

【０００５】本発明は上記の課題を解決するためになされたものであり、その目的は、貫通転位の発生を抑制したIII族窒化物系化合物半導体を製造することである。

【０００６】

【課題を解決するための手段】上記の課題を解決するため、請求項１に記載の発明は、基板上にIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、基板表面の少なくとも一部を削り、基板面に段差を設ける工程と、基板の、削られなかった表面に点状、ストライプ状又は格子状等の島状態に形成された上面を核として、所望のIII族窒化物系化合物半導体を、基板の段差の下段上方をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とする。

【０００７】また、請求項２に記載の発明は、基板上にバッファ層を介してIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、基板表面の少なくとも一部を削り、基板面に段差を設ける工程と、バッファ層を基板に形成する工程と、基板の、削られなかった表面に点状、ストライプ状又は格子状等の島状態に形成されたバッファ層を核として、所望のIII族窒化物系化合物半導体を、基板の段差の下段上方をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とする。

【０００８】また、請求項３に記載の発明は、基板上にバッファ層を介してIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、基板表面の少なくとも一部を削り、基板面に段差を設ける工程と、バッファ層を基板に形成する工程と、バッファ層上にIII族窒化物系化合物半導体を縦方向エピタキシャル成長させて単結晶層を形成する工程と、基板の、削られなかった表面に点状、ストライプ状又は格子状等の島状態に形成されたバッファ層上のIII族窒化物系化合物半導体の単結晶層を核として、所望のIII族窒化物系化合物半導体を、基板の段差の下段上方をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とする。

【０００９】また、請求項４に記載の発明は、基板上にバッファ層を介してIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、バッファ層を基板に形成する工程と、バッファ層と基板表面の少なくとも一部を削り、基板面にバッファ層の形成された上段と、バッファ層の形成されていない下段との段差を設ける工程と、基板の、削られなかった表面に点状、ストライプ状又は格子状等の島状態に形成されたバッファ層を核として、所望のIII族窒化物系化合物半導体を、基板の段差の下段上方をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とする。

【００１０】また、請求項５に記載の発明は、基板上にバッファ層を介してIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、バッファ層を基板に形成する工程と、バッファ層上にIII族窒化物系化合物半導体を縦方向エピタキシャル成長させて単結晶層を形成する工程と、III族窒化物系化合物半導体の単結晶層とバッファ層と基板表面の少なくとも一部を削り、基板面にIII族窒化物系化合物半導

体の単結晶層及びバッファ層の形成された上段と、III族窒化物系化合物半導体の単結晶層とバッファ層の形成されていない下段との段差を設ける工程と、基板の、削られなかった表面に点状、ストライプ状又は格子状等の島状態に形成されたバッファ層上のIII族窒化物系化合物半導体の単結晶層を核として、所望のIII族窒化物系化合物半導体を、基板の段差の下段上方をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とする。

【００１１】また、請求項６に記載の発明は、基板上にIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、基板表面の少なくとも一部の平滑度を悪化させ、III族窒化物系化合物半導体層が充分には形成されない部分を基板表面に形成する表面処理工程と、III族窒化物系化合物半導体を基板に形成し、III族窒化物系化合物半導体の単結晶層が充分に形成された部分と、III族窒化物系化合物半導体の単結晶層が充分には形成されていない部分とを形成する工程と、基板の平滑度を悪化させていない部分に、点状、ストライプ状又は格子状等の島状態に形成されたIII族窒化物系化合物半導体の単結晶層を核として、III族窒化物系化合物半導体を、III族窒化物系化合物半導体の単結晶層が充分には形成されていない部分をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とする。

【００１２】また、請求項７に記載の発明は、基板上にバッファ層を介してIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、基板表面の少なくとも一部の平滑度を悪化させ、バッファ層が充分には形成されない部分を基板表面に形成する表面処理工程と、バッファ層を基板に形成し、バッファ層が充分に形成された部分と、バッファ層が充分には形成されていない部分とを形成する工程と、基板の平滑度を悪化させていない部分に、点状、ストライプ状又は格子状等の島状態に形成されたバッファ層を核として、所望のIII族窒化物系化合物半導体を、バッファ層が充分には形成されていない部分をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とする。

【００１３】また、請求項８に記載の発明は、基板上にバッファ層を介してIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、基板表面の少なくとも一部の平滑度を悪化させ、バッファ層が充分には形成されない部分を基板表面に形成する表面処理工程と、バッファ層を基板に形成し、バッファ層が充分に形成された部分と、バッファ層が充分には形成されていない部分とを形成する工程と、バッファ層が充分に形成された部分にIII族窒化物系化合物半導体の単結晶層を形成する工程と、基板の平滑度を悪化させていない部分に形成された、点状、ストライプ状又は格子状等の島状態のバッファ層上のIII族窒化物系化合物半導体の単結晶層を核として、所望のIII族窒化物系化合物半導体を、バッファ層が充分には形成されていない部分をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とする。

【００１４】また、請求項９に記載の発明は、基板上にバッファ層を介してIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、バッファ層を基板に形成する工程と、バッファ層表面の少なくとも一部の平滑度を悪化させ、III族窒化物系化合物半導体の単結晶層が充分には形成されない部分を形成する表面処理工程と、平滑度を悪化させていない部分の、点状、ストライプ状又は格子状等の島状態のバッファ層を核として、所望のIII族窒化物系化合物半導体を、バッファ層の平滑度を悪化させた部分をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とする。

【００１５】また、請求項１０に記載の発明は、基板上にバッファ層を介してIII族窒化物系化合物半導体を成長させるIII族窒化物系化合物半導体の製造方法において、バッファ層を基板に形成する工程と、第１のIII族窒化物系化合物半導体をバッファ層上に形成する工程と、第１のIII族窒化物系化合物半導体表面の少なくとも一部の平滑度を悪化させ、第２のIII族窒化物系化合物半導体の単結晶層が充分には形成されない部分を形成する表面処理工程と、平滑度を悪化させていない部分の、点状、ストライプ状又は格子状等の島状態の第１のIII族窒化物系化合物半導体を核として、第２のIII族窒化物系化合物半導体を、バッファ層の平滑度を悪化させて部分をも覆うよう、縦及び横方向エピタキシャル成長させる工程とを有することを特徴とする。

【００１６】また、請求項１１に記載の発明は、請求項１乃至請求項１０のいずれか１項に記載のIII族窒化物系化合物半導体の製造方法により製造したIII族窒化物系化合物半導体層の、横方向エピタキシャル成長した部分の上層に形成されたことを特徴とするIII族窒化物系化合物半導体素子である。

【００１７】また、請求項１２に記載の発明は、請求項１乃至請求項１０のいずれか１項に記載のIII族窒化物系化合物半導体の製造方法により製造したIII族窒化物系化合物半導体層の、横方向エピタキシャル成長した部分の上層に、異なるIII族窒化物系化合物半導体層を積層することにより得られることを特徴とするIII族窒化物系化合物半導体発光素子である。

【００１８】また、請求項１３に記載の発明は、請求項１乃至請求項１０のいずれか１項に記載のIII族窒化物系化合物半導体の製造方法に加えて、横方向エピタキシャル成長した部分の上層以外を略全部除去することにより、III族窒化物系化合物半導体基板を得ることを特徴とする。

【0019】
【作用及び発明の効果】本発明のIII族窒化物系化合物半導体の製造方法の概略を、図1乃至図11を参照しながら説明する。
【0020】〔請求項1、2、3の発明〕図1の（a）のように、基板1を、ストライプ状又は格子状等の島状態に削り、段差を設ける。次にバッファ層2を形成する。以下、図1の（b）のように、バッファ層2が、主に基板1の段差の上段面に形成される部分21と段差の下段面に形成される部分22とから成る場合を説明する。
【0021】図1の（b）のような、ストライプ状又は格子状等の島状態の段差を有する基板1の、段差の上段面に形成される部分21と段差の下段面に形成される部分22とからなるバッファ層2を核としてIII族窒化物系化合物半導体3を縦及び横方向エピタキシャル成長させる。すると、図1（c）のように、段差の下段面に形成されたバッファ層22から成長するIII族窒化物系化合物半導体32が段差を埋める前に、段差の上段面に形成されたバッファ層21を核として成長するIII族窒化物系化合物半導体31が段差上方を覆う様にすることができる。さらにIII族窒化物系化合物半導体3を縦及び横方向成長させれば、図1の（d）のように、基板の段差の上方は、横方向エピタキシャル成長により覆われるので、縦方向に伝搬する貫通転位の密度が極めて少なくなる。
【0022】このとき、段差の下段の底面に形成されたバッファ層22から縦方向にエピタキシャル成長するIII族窒化物系化合物半導体32が段差の上段まで成長するよりも、段差の上段面に形成されたバッファ層21から横方向にエピタキシャル成長するIII族窒化物系化合物半導体31が向かい合う段差の上段面からの横方向エピタキシャル成長面と合体する方が早いならば、段差を埋めた部分のIII族窒化物系化合物半導体31上部には段差の底面に形成されたバッファ層22から伝搬する貫通転位は著しく抑制され、極めて良質な結晶領域とすることができる。この場合、図1の（d）のように段差の底面に形成されたバッファ層22を核として成長したIII族窒化物系化合物半導体32の成長面が表面に出ることなく空洞として残ることとなる。その上部は両側の段差の上段面に形成されたバッファ層21を核として成長したIII族窒化物系化合物半導体31の成長面の合体が生じており、バッファ層22から伝搬する貫通転位はこの空洞で止められることとなる。
【0023】次に、図1の（b）のような基板1の段差の側面にバッファ層がほとんど形成されない場合ではなく、基板1の段差の側面にもバッファ層が形成される場合を図2で説明する。図1（a）同様、基板1を削って段差を形成する（図2の（a））。図2の（b）のように、ストライプ状又は格子状等の島状態の段差を有する基板1の、段差の上段面、段差の下段面、及び段差の側面に形成されるバッファ層2を核としてIII族窒化物系化合物半導体3を縦及び横方向エピタキシャル成長させる。すると、図2（c）のように、段差の下段面、及び側面のバッファ層2から縦方向成長するIII族窒化物系化合物半導体3が段差を埋めるとともに、段差の上段面のバッファ層2から横方向成長するIII族窒化物系化合物半導体3も段差を覆う様に成長する。尚、ここで段差の側面から「縦」方向に成長するとは段差の側面の法線方向の成長を言う。すると、図1の（d）のように、基板の段差の上方は、段差の側面のバッファ層2から縦方向成長するIII族窒化物系化合物半導体3が段差を埋める部分と、段差の上段面のバッファ層2から横方向成長するIII族窒化物系化合物半導体3とでしめられる。段差の側面のバッファ層2から縦方向成長するIII族窒化物系化合物半導体3の縦方向の貫通転位は段差の側面の法線方向であり、基板面（上段面及び底面）から縦方向に伝搬する貫通転位の密度が極めて少なくなる。
【0024】このとき、段差の下段の底面に形成されたバッファ層2から縦方向にエピタキシャル成長するIII族窒化物系化合物半導体3が段差の上段まで成長するよりも、段差の上段面に形成されたバッファ層2から横方向にエピタキシャル成長するIII族窒化物系化合物半導体3が向かい合う段差の上段面からの横方向エピタキシャル成長面と合体する方が早いならば、段差を埋めた部分のIII族窒化物系化合物半導体3上部には段差の底面に形成されたバッファ層2から伝搬する貫通転位は著しく抑制され、極めて良質な結晶領域とすることができる。この場合、図2の（d）のように段差の底面に形成されたバッファ層2を核として成長したIII族窒化物系化合物半導体3の成長面が表面に出ることなく空洞として残ることとなる。その上部は両側の段差の上段面に形成されたバッファ層2を核として成長したIII族窒化物系化合物半導体3の成長面の合体が生じており、バッファ層2から伝搬する貫通転位はこの空洞で止められることとなる
【0025】上記の様な速い横方向エピタキシャル成長は、III族窒化物系化合物半導体層31が｛11－20｝面を段差側面方向の成長面とするとき容易に実現可能である。このとき例えば横方向エピタキシャル成長中の成長面の少なくとも上部を｛11－20｝面のまま保てば良い。勿論、横方向エピタキシャル成長面はIII族窒化物系化合物半導体層の｛11－20｝面に限定されない。
【0026】以上のようなことは、バッファ層を要せずに基板に直接エピタキシャル成長するIII族窒化物系化合物半導体にも応用できる。これを図3に示す。基板1を削って段差を形成したのち（図3の（a））、III族窒化物系化合物半導体3を縦及び横方向成長させ（図3の（b））、段差の上段面に形成される部分のIII族窒

化物系化合物半導体３を核とした横方向成長により段差を覆う（図3の（ｃ））。また、図4に示すように、バッファ層２（段差の上段のバッファ層２１と段差の下段のバッファ層２２）にIII族窒化物系化合物半導体の単結晶層３（段差の上段の単結晶層３１と段差の下段の単結晶層３２）を形成して（図4の（ｂ））、段差の上段の単結晶層３１を核とした横方向成長により段差を覆うこともできる（図4の（ｃ）、（ｄ））。

【００２７】〔請求項4、5の発明〕図5の（ａ）のように、基板１上にバッファ層２を形成する。次に図5の（ｂ）のように、バッファ層２と基板１を削り、段差を設ける。ここで図5の（ｃ）のように、III族窒化物系化合物半導体３１を主にバッファ層２を核として縦及び横方向エピタキシャル成長させる。図5の（ｃ）では段差の底面及び側面からも一部III族窒化物系化合物半導体３２のエピタキシャル成長が起こった場合を示している。このとき、段差の下段の底面及び側面からエピタキシャル成長するIII族窒化物系化合物半導体３２が段差の上段まで成長するよりも、段差の上段面に形成されたバッファ層２から横方向にエピタキシャル成長するIII族窒化物系化合物半導体３１が向かい合う段差の上段面からの横方向エピタキシャル成長面と合体する方が早いならば、段差を埋めた部分のIII族窒化物系化合物半導体３１上部には段差の底面から伝搬する貫通転位は著しく抑制され、極めて良質な結晶領域とすることができる。この場合、図5の（ｄ）のように段差の底面から成長したIII族窒化物系化合物半導体３２の成長面が表面に出ることなく空洞として残ることとなる。その上部は両側の段差の上段面に形成されたバッファ層２を核として成長したIII族窒化物系化合物半導体３１の成長面の合体が生じており、バッファ層２から伝搬する貫通転位はこの空洞で止められることとなる。

【００２８】上記の様な速い横方向エピタキシャル成長は、III族窒化物系化合物半導体層３１が｛１１－２０｝面を段差側面方向の成長面とするとき容易に実現可能である。このとき例えば横方向エピタキシャル成長中の成長面の少なくとも上部を｛１１－２０｝面のまま保てば良い。勿論、横方向エピタキシャル成長面はIII族窒化物系化合物半導体層の｛１１－２０｝面に限定されない。

【００２９】また、図6に示すように、バッファ層２とIII族窒化物系化合物半導体の単結晶層３１を形成して（図6の（ａ））、段差を形成し（図6の（ｂ））、段差の上段の単結晶層３１を核とした横方向成長により段差を覆うこともできる（図6の（ｃ）、（ｄ））。

【００３０】〔請求項6、7、8の発明〕図7の（ａ）のように、基板１表面に例えばエッチング、罫描きなどにより荒れた部分Ａを形成し、荒れていない部分がストライプ状又は格子状等の島状態となるようにする。ここにバッファ層２を形成すると、表面の荒れていない部分に形成されたバッファ層２１と比較し、表面の荒れた部分Ａに形成されるバッファ層２２は表層に均一な結晶層ができず、且つ成長速度が遅い（図7の（ｂ））。ここにIII族窒化物系化合物半導体３を縦及び横方向エピタキシャル成長させると、主に表面の荒れていない部分に形成されたバッファ層２１を核として単結晶層が速い速度で形成され、表面の荒れた部分Ａに形成されるバッファ層２２をも横方向に成長することで覆っていく（図7の（ｃ））。更にIII族窒化物系化合物半導体３の縦及び横方向エピタキシャル成長を続けると、表面の荒れた部分Ａに形成されるバッファ層２２は、主に表面の荒れていない部分に形成されたバッファ層２１を核として横方向エピタキシャル成長したIII族窒化物系化合物半導体３が完全に覆うこととなる。このとき、表面の荒れた部分Ａに形成されるバッファ層２２からの縦方向の貫通転位は、その上方に横方向エピタキシャル成長により形成されたIII族窒化物系化合物半導体３には伝搬しないこととなる。

【００３１】図8の（ａ）のように、基板１表面に例えばエッチング、罫描きなどにより荒れた部分Ａを形成し、荒れていない部分がストライプ状又は格子状等の島状態となるようにする。基板１上にエピタキシャル成長するIII族窒化物系化合物半導体３をここに形成すると、表面の荒れていない部分に形成されたIII族窒化物系化合物半導体層３１と比較し、表面の荒れた部分Ａに形成されるIII族窒化物系化合物半導体層３２は表層に均一な単結晶層ができず、且つ成長速度が遅い（図8の（ｂ））。III族窒化物系化合物半導体３を縦及び横方向エピタキシャル成長させる条件でエピタキシャル成尿を続ければ、表面の荒れた部分Ａに形成されるIII族窒化物系化合物半導体層３２上部は、主に表面の荒れていない部分に形成されたIII族窒化物系化合物半導体３１が横方向エピタキシャル成長して完全に覆うこととなる。このとき、表面の荒れた部分Ａに形成されるIII族窒化物系化合物半導体３２からの縦方向の貫通転位は、その上方に横方向エピタキシャル成長により形成されたIII族窒化物系化合物半導体３１には伝搬しないこととなる。

【００３２】更には、図9のように、図7のようなIII族窒化物系化合物半導体３の１段の縦及び横方向エピタキシャル成長ではなく、まず表面の荒れていない部分に形成されたバッファ層２１上にIII族窒化物系化合物半導体３１を縦方向成長させて単結晶層とし、次にこのIII族窒化物系化合物半導体３１の単結晶層を核としてIII族窒化物系化合物半導体３２を縦及び横方向成長させることもできる。

【００３３】〔請求項9、10の発明〕図10のように、基板１にバッファ層２を形成したのち（図10の（ａ））、その表面をエッチング、罫描きにより表面を悪化させ（図10の（ｂ））、III族窒化物系化合物半

導体３を縦及び横方向成長させても良い（図１０の（ｃ）、（ｄ））。また、図１１のように、基板１にバッファ層２とIII族窒化物系化合物半導体層３１を形成したのち（図１１の（ａ））、その表面をエッチング、罫描きにより表面を悪化させ（図１１の（ｂ））、III族窒化物系化合物半導体３３を縦及び横方向成長させても良い（図１１の（ｃ）、（ｄ））。いずれも、表面が悪化していない部分により早くIII族窒化物系化合物半導体層が形成されるのでそれを核として横方向成長させることにより、表面が悪化した部分をも覆うよう成長させることができる。

【００３４】以上のような方法により、縦方向に伝搬する貫通転位を抑制した領域を有するIII族窒化物系化合物半導体を形成することができる。

【００３５】上記の工程で得られたIII族窒化物系化合物半導体層の、横方向エピタキシャル成長した部分の上層に素子を形成することで、欠陥の少ない、移動度の大きい層を有する半導体素子とすることができる（請求項１１）。

【００３６】上記の工程で得られたIII族窒化物系化合物半導体層の、横方向エピタキシャル成長した部分の上層に発光素子を形成することで、素子寿命、或いはＬＤの閾値の改善された発光素子とすることができる（請求項１２）。

【００３７】また、上記の工程で得られたIII族窒化物系化合物半導体層の、横方向エピタキシャル成長した部分の上層のみをその他の層から分離することで、転位等結晶欠陥の著しく抑制された結晶性の良いIII族窒化物系化合物半導体を得ることができる（請求項１３）。尚「略全部除去」とは、製造上の簡便さから、一部貫通転位の残った部分を含んでいたとしても本発明に包含されることを示すものである。

【００３８】

【発明の実施の形態】図１乃至図８に本発明のIII族窒化物系化合物半導体の製造方法の実施の形態のそれぞれの一例の概略を示す。図１においては、バッファ層２が基板１のダイシングにより形成された側面に形成されない例を示している。基板１をダイシングして段差を形成し（図１の（ａ））、バッファ層２を形成して（図１の（ｂ））、III族窒化物系化合物半導体層３を横方向エピタキシャル成長させる（図１の（ｃ））。図１の（ａ）のダイシングの幅と深さは、上述のように段差の底面に形成されたバッファ層２２を核として縦方向成長するIII族窒化物系化合物半導体層３２が段差を埋める前に、段差の上段面に形成されたバッファ層２１を核として縦及び横方向成長するIII族窒化物系化合物半導体層３１が段差の上部を覆うよう決定される。図１の（ｃ）では横方向エピタキシャル成長面が例えば｛１１－２０｝面である場合を想定しているが、本発明は成長面に限定されない。こうして、段差の底面の縦方向の成長によりダイシングされた部分が埋まる前に、段差の上段面に形成されたバッファ層２１を核として横方向成長がダイシングされた部分の上方で合体するよう、ダイシング形状と横方向エピタキシャル成長条件とを設定することで、ダイシングされた上部のIII族窒化物系化合物半導体３１には貫通転位が抑制された領域を形成する（図１の（ｄ））。

【００３９】図２は基板１の段差の側面にもバッファ層２が形成される場合を示す。これも図１の場合とほぼ同様である。

【００４０】図５は基板１にバッファ層２を形成したのちダイシングする実施の形態である。バッファ層２が形成されていない基板１の段差の底面及び側面での縦方向成長は無いか極めて遅く、段差の上段面に形成されたバッファ層２を核とした横方向成長によりダイシングされた段差を覆う（図５の（ｃ）及び（ｄ））。図２の（ａ）のダイシングの幅と深さは、上述のように段差の底面から縦方向成長するIII族窒化物系化合物半導体層３２が段差を埋める前に、段差の上段面に形成されたバッファ層２１を核として縦及び横方向成長するIII族窒化物系化合物半導体層３１が段差の上部を覆うよう決定される。図２の（ｃ）では横方向エピタキシャル成長面が例えば｛１１－２０｝面である場合を想定しているが、本発明は成長面に限定されない。

【００４１】図７は、基板１の表面を荒らしたのちバッファ層２を形成する実施の形態である。表面の荒れた部分Ａの面積等は、荒れた部分Ａ上に形成された、表層に均一な単結晶層ができず且つ成長速度が遅いバッファ層２２上を、面の荒れていない部分に形成されたバッファ層２１を核としたIII族窒化物系化合物半導体３が縦及び横方向エピタキシャル成長して覆うよう決定される。

【００４２】図８は、基板１の表面を荒らしたのちIII族窒化物系化合物半導体を直接形成する実施の形態である。表面の荒れた部分Ａの面積等は、荒れた部分Ａ上に形成された、表層に均一な単結晶層ができず且つ成長速度が遅いIII族窒化物系化合物半導体３２上を、面の荒れていない部分に形成されたIII族窒化物系化合物半導体層３１が縦及び横方向エピタキシャル成長して覆うよう決定される。

【００４３】上記の発明の実施の形態としては、次の中からそれぞれ選択することができる。

【００４４】基板上にIII族窒化物系化合物半導体を順次積層を形成する場合は、基板としてはサファイア、シリコン(Si)、炭化ケイ素(SiC)、スピネル($MgAl_2O_4$)、ZnO、MgOその他の無機結晶基板、リン化ガリウム又は砒化ガリウムのようなIII-V族化合物半導体あるいは窒化ガリウム(GaN)その他のIII族窒化物系化合物半導体等を用いることができる。

【００４５】III族窒化物系化合物半導体層を形成する方法としては有機金属気相成長法（MOCVD又はMOVPE）が

好ましいが、分子線気相成長法（MBE）、ハライド気相成長法（Halide VPE）、液相成長法（LPE）等を用いても良く、各層を各々異なる成長方法で形成しても良い。

【００４６】例えばサファイア基板上にIII族窒化物系化合物半導体積層する際、結晶性良く形成させるため、サファイア基板との格子不整合を是正すべくバッファ層を形成することが好ましい。他の基板を使用する場合もバッファ層を設けることが望ましい。バッファ層としては、低温で形成させたIII族窒化物系化合物半導体$Al_xGa_yIn_{1-x-y}N$（$0 \leqq x \leqq 1$, $0 \leqq y \leqq 1$, $0 \leqq x+y \leqq 1$）、より好ましくは$Al_xGa_{1-x}N$（$0 \leqq x \leqq 1$）が用いられる。このバッファ層は単層でも良く、組成等の異なる多重層としても良い。バッファ層の形成方法は、380～420℃の低温で形成するものでも良く、逆に1000～1180℃の範囲で、ＭＯＣＶＤ法で形成しても良い。また、ＤＣマグネトロンスパッタ装置を用いて、高純度金属アルミニウムと窒素ガスを原材料として、リアクティブスパッタ法によりAlNから成るバッファ層を形成することもできる。同様に一般式$Al_xGa_yIn_{1-x-y}N$（$0 \leqq x \leqq 1$, $0 \leqq y \leqq 1$, $0 \leqq x+y \leqq 1$、組成比は任意）のバッファ層を形成することができる。更には蒸着法、イオンプレーティング法、レーザアブレーション法、ＥＣＲ法を用いることができる。物理蒸着法によるバッファ層は、200～600℃で行うのが望ましい。さらに望ましくは300～500℃であり、さらに望ましくは350～450℃である。これらのスパッタリング法等の物理蒸着法を用いた場合には、バッファ層の厚さは、100～3000Åが望ましい。さらに望ましくは、100～500Åが望ましく、最も望ましくは、100～300Åである。また、横方向エピタキシャル成長の成長の核となるIII族窒化物系化合物半導体層及び／又は上層のIII族窒化物系化合物半導体は、バッファ層と単結晶III族窒化物系化合物半導体層とを１周期として、多重周期形成した層（基底層）としても良い。また、基底層を用いる場合は、横方向エピタキシャル成長の核となる層として、最上層は単結晶層がより望ましい。

【００４７】バッファ層、横方向エピタキシャル成長の成長の核となるIII族窒化物系化合物半導体層、横方向エピタキシャル成長させる層、及び／又は上層のIII族窒化物系化合物半導体は、III族元素の組成の一部は、ボロン(B)、タリウム(Tl)で置き換えても、また、窒素(N)の組成一部をリン(P)、ヒ素(As)、アンチモン(Sb)、ビスマス(Bi)で置き換えても本発明を実質的に適用できる。また、これら元素を組成に表示できない程度のドープをしたものでも良い。例えば組成にインジウム(In)、ヒ素(As)を有しないIII族窒化物系化合物半導体である$Al_xGa_{1-x}N$（$0 \leqq x \leqq 1$）に、アルミニウム(Al)、ガリウム(Ga)よりも原子半径の大きなインジウム(In)、又は窒素(N)よりも原子半径の大きな(As)をドープすることで、窒素原子の抜けによる結晶の拡張歪みを圧縮歪みで補償し結晶性を良くしても良い。この場合はアクセプタ不純物がIII族原子の位置に容易に入るため、ｐ型結晶をアズグローンで得ることもできる。このようにして結晶性を良くすることで本願発明と合わせて更に貫通転位を１００乃至１０００分の１程度にまで下げることもできる。なお、発光素子として構成する場合は、本来III族窒化物系化合物半導体の２元系、若しくは３元系を用いることが望ましい。

【００４８】ｎ型のIII族窒化物系化合物半導体層を形成する場合には、ｎ型不純物として、Si、Ge、Se、Te、C等IV族元素又はVI族元素を添加することができる。また、ｐ型不純物としては、Zn、Mg、Be、Ca、Sr、Ba等II族元素又はIV族元素を添加することができる。これらを複数或いはｎ型不純物とｐ型不純物を同一層にドープしても良い。

【００４９】横方向エピタキシャル成長としては成長面が基板に垂直となるものが望ましいが、基板に対して斜めのファセット面のまま成長するものでも良い。

【００５０】横方向エピタキシャル成長としては、横方向エピタキシャル成長面の少なくとも上部と基板面とは垂直であることがより望ましく、更にはいずれもIII族窒化物系化合物半導体の｛１１－２０｝面であることがより望ましい。

【００５１】エッチングする際は、深さと幅の関係から、横方向エピタキシャル成長により塞がれるように段差を設ける。この時、異なる層からの縦方向成長が少なくとも初期段階において遅いことも利用する。

【００５２】基板上に積層するIII族窒化物系化合物半導体層の結晶軸方向が予想できる場合は、基板の段差側面がIII族窒化物系化合物半導体層のａ面（｛１１－２０｝面）又はm面（｛１－１００｝面）と平行となるようストライプ状にマスク或いはダイシングを施すことが有用である。なお、島状、格子状等に、上記ストライプ及びマスクを任意に設計して良い。横方向エピタキシャル成長面は、基板面に垂直なものの他、基板面に対し斜めの角度の成長面でも良い。III族窒化物系化合物半導体層のａ面として（１１－２０）面を横方向エピタキシャル成長面とするには例えばストライプの長手方向はIII族窒化物系化合物半導体層のm面である（１－１００）面に垂直とする。例えば基板をサファイアのａ面又はｃ面とする場合は、どちらもサファイアのm面がその上に形成されるIII族窒化物系化合物半導体層のａ面と通常一致するので、これに合わせてダイシングを施す。点状、格子状その他の島状とする場合も、輪郭（側壁）を形成する各面が上方に形成されるIII族窒化物系化合物半導体層の｛１１－２０｝面と一致することが望ましい。

【００５３】エッチングマスクは、酸化珪素(SiO_2)、窒化珪素(Si_3N_4)、酸化チタン(TiO_X)、酸化ジルコニウム(ZrO_X)等の酸化物、窒化物、これらの多層膜をもちいることができる。これらの成膜方法は蒸着、スパッタ、Ｃ

ＶＤ等の気相成長法の他、任意である。

【００５４】エッチングをする場合は反応性イオンビームエッチング（ＲＩＢＥ）が望ましいが、任意のエッチング方法を用いることができる。また、エッチングに代えて、スクライビング等、機械的方法により段差を形成しても良い。表面を荒らす場合も、スクライビング、ダイヤモンドカッターによる罫描き等、任意である。

【００５５】上記の貫通転位の抑制された領域を有するIII族窒化物系化合物半導体の、全体或いは貫通転位の抑制された領域を中心としてその上部にＦＥＴ、発光素子等の半導体素子を形成することができる。発光素子の場合は、発光層は多重量子井戸構造（ＭＱＷ）、単一量子井戸構造（ＳＱＷ）の他、ホモ構造、ヘテロ構造、ダブルヘテロ構造のものが考えられるが、ｐｉｎ接合或いはｐｎ接合等により形成しても良い。

【００５６】上述の、貫通転位の抑制された領域を有するIII族窒化物系化合物半導体を、例えば基板１、バッファ層２及びダイシングにより段差を設けた貫通転位の抑制されていない部分を除去して、III族窒化物系化合物半導体基板とすることができる。この上にIII族窒化物系化合物半導体素子を形成することが可能であり、或いはより大きなIII族窒化物系化合物半導体結晶を形成するための基板として用いることができる。除去方法としては、メカノケミカルポリッシングの他、任意である。

【００５７】本発明の適用として、基板処理により貫通転位の少ない領域を形成したのち、更に横方向エピタキシャル成長を利用して、貫通転位の多い領域上部に貫通転位の少ない領域を形成することも本発明に包含される。例えば本発明の請求項１乃至請求項４の手段により貫通転位の少ない領域と多い領域を有するIII族窒化物系化合物半導体層の、貫通転位の多い領域にマスクを形成し、マスクを形成していない貫通転位の少ない領域表面を核としてマスク上部を横方向エピタキシャル成長により覆うことで、全体として貫通転位の少ないIII族窒化物系化合物半導体層を得ることができる。その他、貫通転位の多い領域上部での第２の横方向エピタキシャル成長は任意である。

【００５８】以下、発明の具体的な実施例に基づいて説明する。実施例として発光素子をあげるが、本発明は下記実施例に限定されるものではなく、任意の素子に適用できるの製造方法を開示している。

【００５９】本発明のIII族窒化物系化合物半導体は、有機金属化合物気相成長法（以下「MOVPE」と示す）による気相成長により製造された。用いられたガスは、アンモニア(NH_3)とキャリアガス(H_2又はN_2)とトリメチルガリウム（$Ga(CH_3)_3$，以下「TMG」と記す）とトリメチルアルミニウム（$Al(CH_3)_3$，以下「TMA」と記す）、トリメチルインジウム（$In(CH_3)_3$，以下「TMI」と記す）、シクロペンタジエニルマグネシウム（$Mg(C_5H_5)_2$、以下「Cp_2Mg」と記す）である。

【００６０】〔第１実施例〕有機洗浄及び熱処理により洗浄したａ面を主面とし、単結晶のサファイア基板１をダイシングにより、幅10μｍ、間隔10μｍ、深さ10μｍのストライプ状の段差を形成した。次に、温度を400℃とし、H_2を10L/min、NH_3を5L/min、TMAを20μmol/minで約3分間供給してAlNのバッファ層２を約40nmの厚さに形成した。バッファ層２は基板１の段差の主に上段面と底面に形成された。

【００６１】次に、サファイア基板１の温度を1150℃に保持し、H_2を20L/min、NH_3を10L/min、TMGを5μmol/minで導入して、縦及び横方向エピタキシャル成長によりGaN層３を形成した。この時、主に段差の上段面に形成されたバッファ層２１からの横方向エピタキシャル成長により段差が覆われ、表面が平坦となった（図１の（ｃ））。こののち、H_2を20L/min、NH_3を10L/min、TMGを300μmol/minで導入し、GaN層３を成長させ、10μｍの厚さとした。GaN層３の、基板１の深さ10μｍの段差の底面上方に形成された部分は、段差の上段面上方に形成された部分に比して貫通転位が著しく抑えられた。

【００６２】〔第２実施例〕有機洗浄及び熱処理により洗浄したａ面を主面とし、単結晶のサファイア基板１の温度を400℃とし、H_2を10L/min、NH_3を5L/min、TMAを20μmol/minで約3分間供給してAlNのバッファ層２を約40nmの厚さに形成した。次にダイシングにより、幅10μｍ、間隔10μｍ、深さ10μｍのストライプ状に段差を形成した。バッファ層２は基板１の段差の上段面のみに残った（図５の（ｂ））。

【００６３】次に、サファイア基板１の温度を1150℃に保持し、H_2を20L/min、NH_3を10L/min、TMGを5μmol/minで導入して、縦及び横方向エピタキシャル成長によりGaN層３を形成した。この時、主に段差の上段面に形成されたバッファ層２１からの横方向エピタキシャル成長により段差が覆われ、表面が平坦となった（図５の（ｃ）及び（ｄ））。こののち、H_2を20L/min、NH_3を10L/min、TMGを300μmol/minで導入し、GaN層３を成長させ、10μｍの厚さとした。GaN層３の、基板１の深さ10μｍの段差の底面上方に形成された部分は、段差の上段面上方に形成された部分に比して貫通転位が著しく抑えられた。

【００６４】〔第３実施例〕有機洗浄及び熱処理により洗浄したａ面を主面とし、単結晶のサファイア基板１を反応性イオンビームエッチング（ＲＩＢＥ）を用いた選択ドライエッチングにより、幅10μｍ、間隔10μｍ、ストライプ状に短時間エッチングし、面荒れを起こした。次に、温度を400℃とし、H_2を10L/min、NH_3を5L/min、TMAを20μmol/minで約3分間供給してAlNのバッファ層２を約40nmの厚さに形成した。バッファ層２は面荒れの部分２２と面荒れでない部分２２で表面のモホロジーが異なった（図７の（ｂ））。

【００６５】次に、サファイア基板１の温度を1150℃に

保持し、H_2を20L/min、NH_3を10L/min、TMGを5μmol/minで導入して、縦及び横方向エピタキシャル成長によりGaN層３を形成した。この時、主に面荒れでない部分２１からの横方向エピタキシャル成長により面荒れの部分が覆われ、表面が平坦となった（図７の（ｃ）及び（ｄ））。このち、H_2を20L/min、NH_3を10L/min、TMGを300μmol/minで導入し、GaN層３を成長させ、3μmの厚さとした。GaN層３の、基板１の深さ10μmの段差の底面上方に形成された部分は、段差の上段面上方に形成された部分に比して貫通転位が著しく抑えられた。

【００６６】〔第４実施例〕本実施例では、図１２のようなバッファ層と単結晶III族窒化物系化合物半導体層とを１周期として、多重周期形成した層（基底層）を用いた。有機洗浄及び熱処理により洗浄したａ面を主面とし、単結晶のサファイア基板１上に、温度を400℃まで低下させて、H_2を10L/min、NH_3を5L/min、TMAを20μmol/minで約3分間供給して第１のAlN層２１１を約40nmの厚さに形成した。次に、サファイア基板１の温度を1000℃に保持し、H_2を20L/min、NH_3を10L/min、TMGを300μmol/minで導入し、膜厚約0.3μmのGaN層２１２を形成した。次に温度を400℃まで低下させて、H_2を10L/min、NH_3を5L/min、TMAを20μmol/minで約3分間供給して第２のAlN層２１３を約40nmの厚さに形成した。こうして、膜厚約40nmの第１のAlN層２１１、膜厚約0.3μmのGaN層２１２、膜厚約40nmの第２のAlN層２１３から成る基底層２０を形成した。

【００６７】次に、第２実施例と同様に、ダイシングにより段差を形成した。サファイア基板１のダイシング深さを10μmとした。次に、サファイア基板１の温度を1150℃に保持し、H_2を20L/min、NH_3を10L/min、TMGを5μmol/minで導入し、GaN層３を横方向エピタキシャル成長により形成した。こうして主に段差の上段面に形成された基底層２０を核として横方向エピタキシャル成長により段差が覆われ、表面が平坦となった。こののち、H_2を20L/min、NH_3を10L/min、TMGを300μmol/minで導入し、GaN層３を成長させ、GaN層３を10μmの厚さとした。GaN層３の、サファイア基板１の深さ10μmの段差の底面上方に形成された部分は、段差の上段面上方に形成された部分に比して貫通転位が著しく抑えられた。

【００６８】〔第５実施例〕第１実施例と同様に形成したウエハ上に、図１３のようなレーザダイオード（ＬＤ）１００を次のようにして形成した。但し、GaN層３の形成の際、シラン（SiH_4）を導入して、GaN層３をシリコン(Si)ドープのｎ型GaNから成る層とした。尚、図を簡略とするため、段差を有するサファイア基板１と段差の上段面及び底面に形成されたバッファ層２及び段差を埋めている部分のGaN層３を併せて、ウエハ１０００と記載し、それ以外のGaN層３をGaN層１０３と記載する。

【００６９】段差を有するサファイア基板、AlNから成るバッファ層、その段差を覆うｎ型GaN層から成るウエハ層１０００とｎ型GaN層１０３に、シリコン(Si)ドープの$Al_{0.08}Ga_{0.92}N$から成るｎクラッド層１０４、シリコン(Si)ドープのGaNから成るｎガイド層１０５、ＭＱＷ構造の発光層１０６、マグネシウム(Mg)ドープのGaNから成るｐガイド層１０７、マグネシウム(Mg)ドープの$Al_{0.08}Ga_{0.92}N$から成るｐクラッド層１０８、マグネシウム(Mg)ドープのGaNから成るｐコンタクト層１０９を形成した。次にｐコンタクト層１０９上に金(Au)から成る電極１１０Ａを、２段のGaN層とｎ型GaN層の合計３段のGaN層１０３が露出するまで一部エッチングしてアルミニウム(Al)から成る電極１１０Ｂを形成した。このようにして形成したレーザダイオード（ＬＤ）は素子寿命及び発光効率が著しく向上した。

【００７０】〔第６実施例〕第１実施例と同様に形成したウエハ上に、図１４のような発光ダイオード（ＬＥＤ）２００を次のようにして形成した。但し、GaN層３の形成の際、シラン（SiH_4）を導入して、GaN層３をシリコン(Si)ドープのｎ型GaNから成る層とした。尚、図を簡略とするため、段差を有するサファイア基板１と段差の上段面及び底面に形成されたバッファ層２及び段差を埋めている部分のGaN層３を併せて、ウエハ２０００と記載し、それ以外のGaN層３をGaN層２０３と記載する。

【００７１】サファイア基板、AlNから成るバッファ層、段差を埋めるGaN層から成るウエハ２０００とｎ型GaN層２０３上に、シリコン(Si)ドープの$Al_{0.08}Ga_{0.92}N$から成るｎクラッド層２０４、発光層２０５、マグネシウム(Mg)ドープの$Al_{0.08}Ga_{0.92}N$から成るｐクラッド層２０６、マグネシウム(Mg)ドープのGaNから成るｐコンタクト層２０７を形成した。次にｐコンタクト層２０７上に金(Au)から成る電極２０８Ａを、GaN層とｎ型GaN層の２段のGaN層２０３が露出するまで一部エッチングしてアルミニウム(Al)から成る電極２０８Ｂを形成した。このようにして形成した発光ダイオード（ＬＥＤ）は素子寿命及び発光効率が著しく向上した。

【００７２】〔第７実施例〕本実施例では基板としてシリコン(Si)基板を用いた。シリコン(Si)基板３０１をエッチングにより幅10μm、間隔10μm、深さ10μmのストライプ状にエッチングした。次にシリコン基板３０１の温度を1150℃に保持し、H_2を20L/min、NH_3を10L/min、TMGを5μmol/min、TMAを0.5μmol/min、H_2ガスにより希釈されたたシラン(SiH_4)を0.01μmol/minで供給し、シリコン基板の段差の上段面、側面、底面から$n\text{-}Al_{0.15}Ga_{0.85}N$層を縦及び横方向成長させた。こうして主に上段面を核とする横方向エピタキシャル成長により段差が覆われ、表面が平坦となったのち、H_2を10L/min、NH_3を10L/min、TMGを100μmol/min、TMAを10μmol/min、H_2ガスにより希釈されたたシラン(SiH_4)を0.2μmol/minで供給し、$n\text{-}Al_{0.15}Ga_{0.85}N$層を成長させ、3μmの厚さとし

た。以下、シリコン基板３０１とn-$Al_{0.15}Ga_{0.85}N$層３０２を併せてウエハ３０００と記載する。

【００７３】上記のようにウエハ３０００（段差を有するシリコン基板３０１とその上に形成されたn-$Al_{0.15}Ga_{0.85}N$層３０２）上にシリコン(Si)ドープのGaNから成るｎガイド層３０３、ＭＱＷ構造の発光層３０４、マグネシウム(Mg)ドープのGaNから成るｐガイド層３０５、マグネシウム(Mg)ドープの$Al_{0.08}Ga_{0.92}N$から成るｐクラッド層３０６、マグネシウム(Mg)ドープのGaNから成るｐコンタクト層３０７を形成した。次にｐコンタクト層３０７上に金(Au)から成る電極３０８Ａを、シリコン基板３０１裏面にアルミニウム(Al)から成る電極３０８Ｂを形成した。このようにして形成した図１５のレーザダイオード（ＬＤ）３００は素子寿命及び発光効率が著しく向上した。

【００７４】〔第８実施例〕本実施例でも基板としてシリコン(Si)基板を用いた。第７実施例の段差を有するシリコン基板３０１に形成されたn-$Al_{0.15}Ga_{0.85}N$層３０２と同様に、段差を有するシリコン基板４０１とその上に形成されたn-$Al_{0.15}Ga_{0.85}N$層４０２のウエハ４０００を用意し、発光層４０３、マグネシウム(Mg)ドープの$Al_{0.15}Ga_{0.85}N$から成るｐクラッド層４０４を形成した。次にｐクラッド層４０４上に金(Au)から成る電極４０５Ａを、シリコン基板４０１裏面にアルミニウム(Al)から成る電極４０５Ｂを形成した。このようにして形成した図１６の発光ダイオード（ＬＥＤ）４００は素子寿命及び発光効率が著しく向上した。

【００７５】〔エッチングの変形〕また、図１７は、島状に段差の上段、或いは面荒れ部分Ｂと面荒れを起こさない部分を形成する例である。図１７の（ａ）は、外周をも示しているが、これは理解のため簡略化した模式図であり、実際には島状の段差の上段はウエハ当たり数千万個形成して良い。図１７の（ａ）では、島状の段差の上段に対し、段差の底面Ｂ（或いは面荒れを起こさない部分に対し面荒れ部分Ｂ）は３倍の面積を有する。図１７の（ｂ）では、島状の段差の上段に対し、段差の底面Ｂ（或いは面荒れを起こさない部分に対し面荒れ部分Ｂ）は８倍の面積を有する。

【図面の簡単な説明】

【図１】本発明の第１の実施例に係るIII族窒化物系化合物半導体の製造工程を示す断面図。

【図２】本発明の別のIII族窒化物系化合物半導体の製造工程を示す断面図。

【図３】本発明の第７の実施例に係るIII族窒化物系化合物半導体の製造工程を示す断面図。

【図４】本発明の別のIII族窒化物系化合物半導体の製造工程を示す断面図。

【図５】本発明の第２の実施例に係るIII族窒化物系化合物半導体の製造工程を示す断面図。

【図６】本発明の別のIII族窒化物系化合物半導体の製造工程を示す断面図。

【図７】本発明の第３の実施例に係るIII族窒化物系化合物半導体の製造工程を示す断面図。

【図８】本発明の別のIII族窒化物系化合物半導体の製造工程を示す断面図。

【図９】本発明の更に別のIII族窒化物系化合物半導体の製造工程を示す断面図。

【図１０】本発明の更に別のIII族窒化物系化合物半導体の製造工程を示す断面図。

【図１１】本発明の更に別のIII族窒化物系化合物半導体の製造工程を示す断面図。

【図１２】本発明の第４の実施例に係るIII族窒化物系化合物半導体の製造工程を示す断面図。

【図１３】本発明の第５の実施例に係るIII族窒化物系化合物半導体発光素子の構造を示す断面図。

【図１４】本発明の第６の実施例に係るIII族窒化物系化合物半導体発光素子の構造を示す断面図。

【図１５】本発明の第７の実施例に係るIII族窒化物系化合物半導体発光素子の構造を示す断面図。

【図１６】本発明の第８の実施例に係るIII族窒化物系化合物半導体発光素子の構造を示す断面図。

【図１７】第１のIII族窒化物系化合物半導体のエッチングの他の例を示す模式図。

【図１８】III族窒化物系化合物半導体を伝搬する貫通転位を示す断面図。

【符号の説明】

１、１０１、２０１、３０１、４０１　基板

１０００、２０００、３０００、４０００　段差を有する基板とバッファ層と段差を覆うIII族窒化物系化合物半導体層とから成るウエハ

２　バッファ層

２０　基底層

３１、３２、３３　III族窒化物系化合物半導体

１０３、２０３　n-GaN層

１０４、２０４、３０２、４０２　n-AlGaNクラッド層

１０５、３０３　n-GaNガイド層

１０６、２０５、３０４、４０３　発光層

１０７、３０５　p-GaNガイド層

１０８、２０６、３０６、４０４　p-AlGaNクラッド層

１０９、２０７、３０７　p-GaN層

１１０Ａ、２０８Ａ、３０８Ａ、４０５Ａ　ｐ電極

１１０Ｂ、２０８Ｂ、３０８Ｂ、４０５Ｂ　ｎ電極

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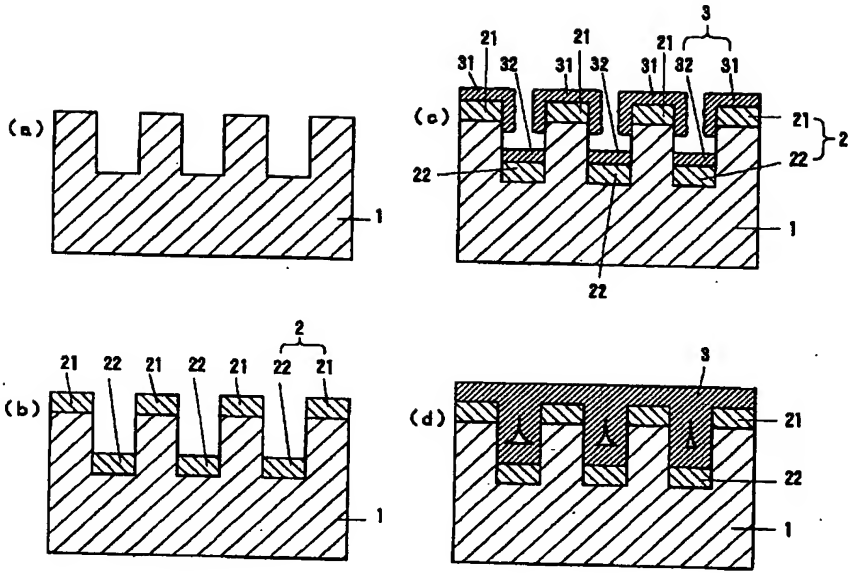

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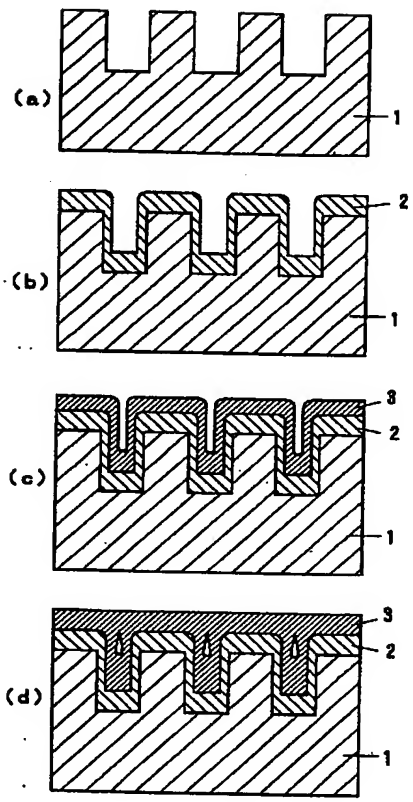

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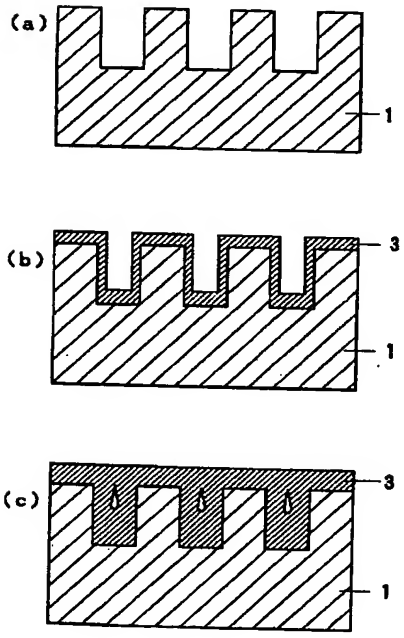

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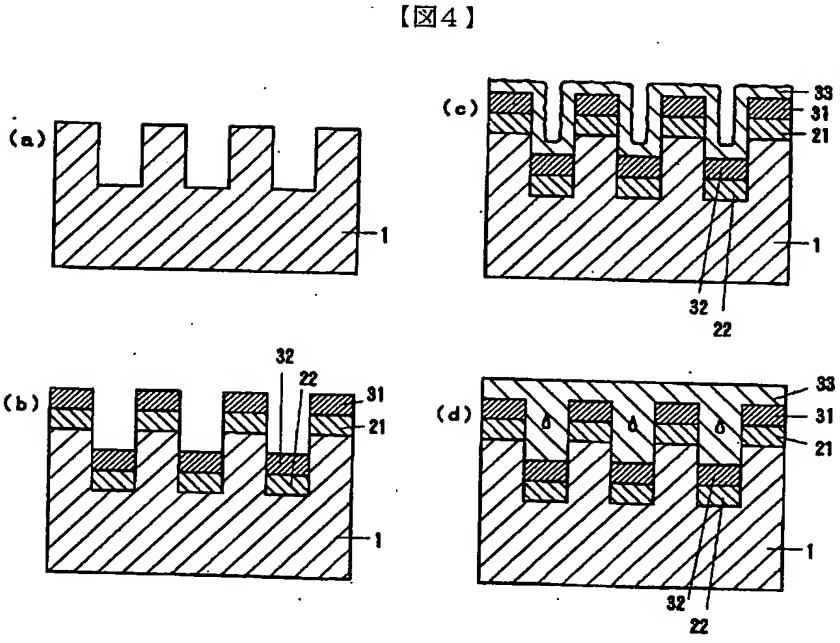

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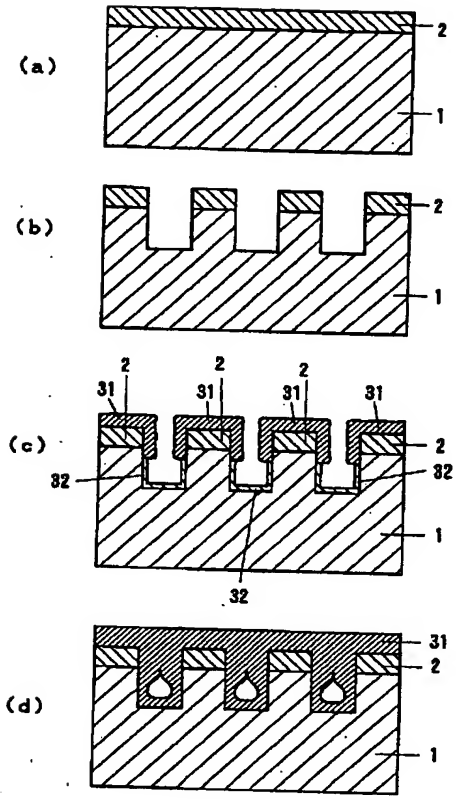
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(b)
2
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(c)
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1
(d)
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2
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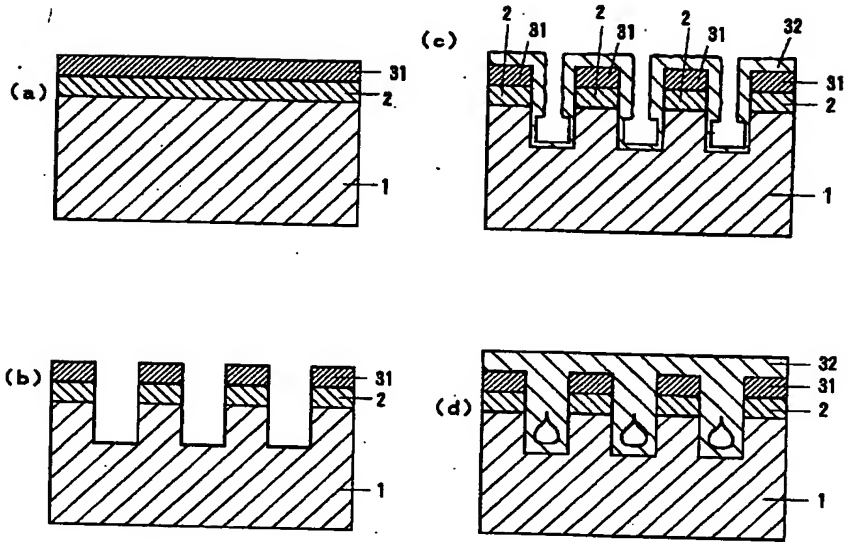
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(c)
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(d)
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2
1

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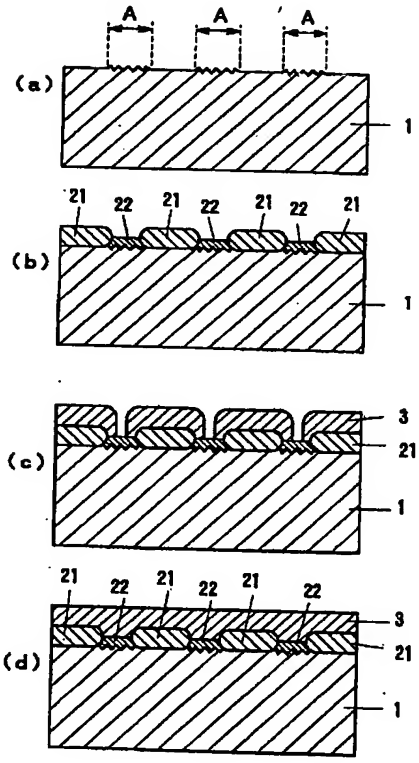
A
(a)
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21
22
(b)
3
(c)
(d)

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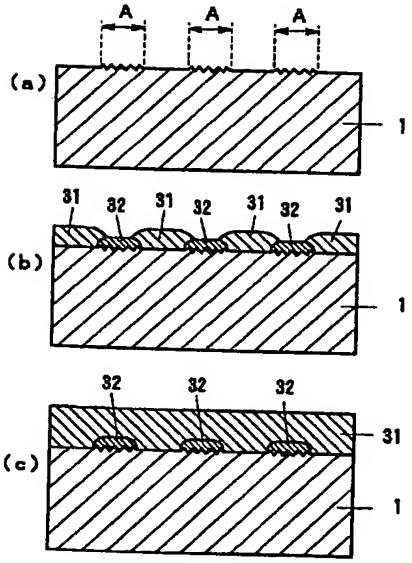
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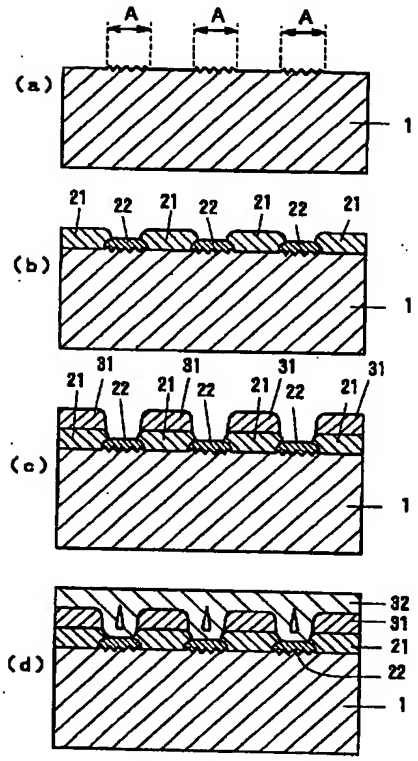
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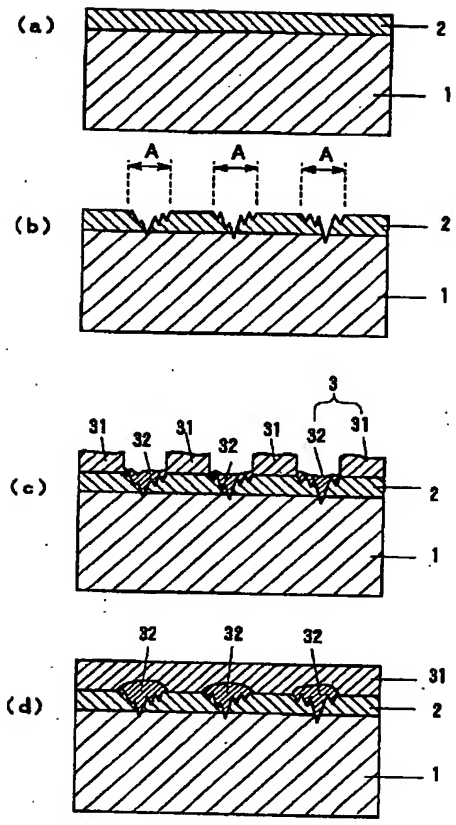
22
1
(d)

【図10】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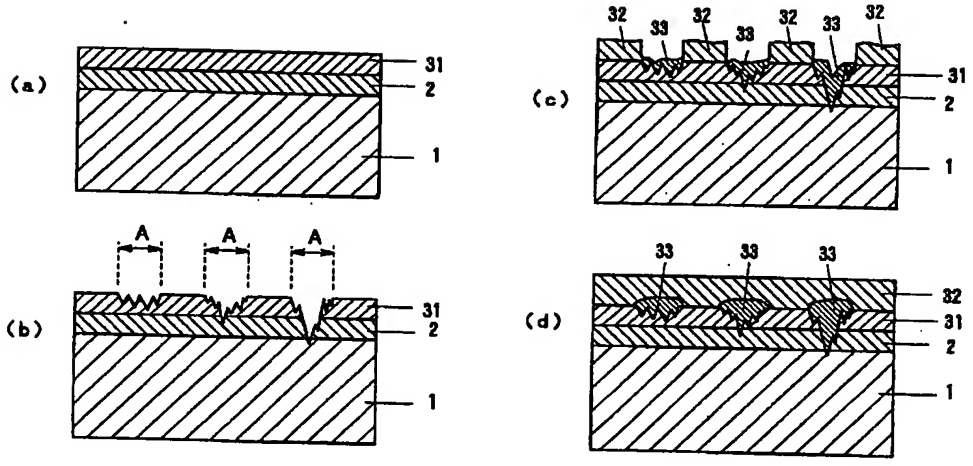
32
31
(d)
2
1

【図11】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32
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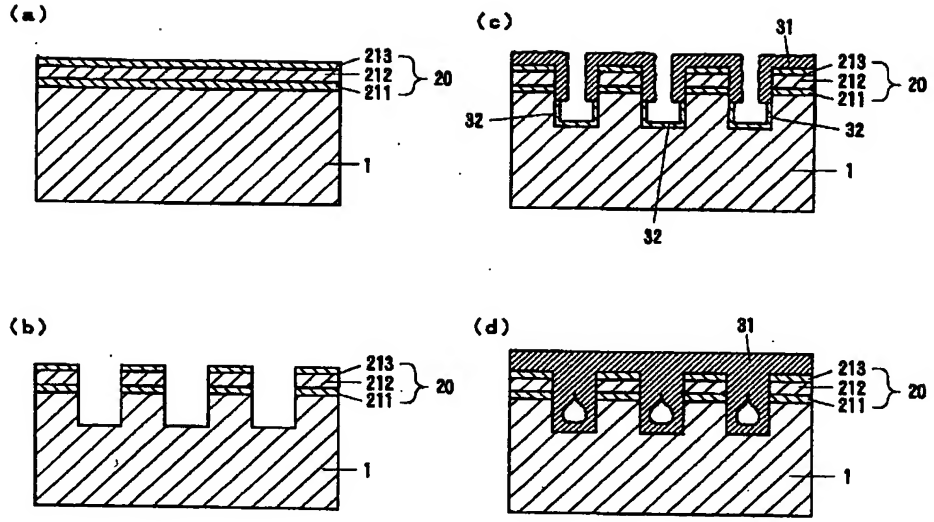
2
1

【図12】


(a)
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212
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20
1

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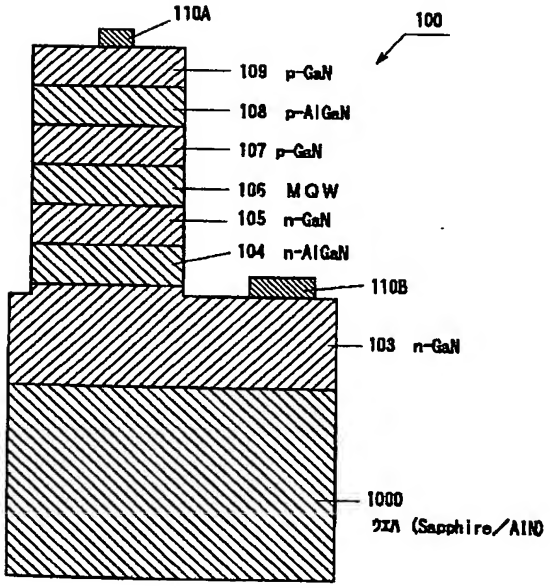
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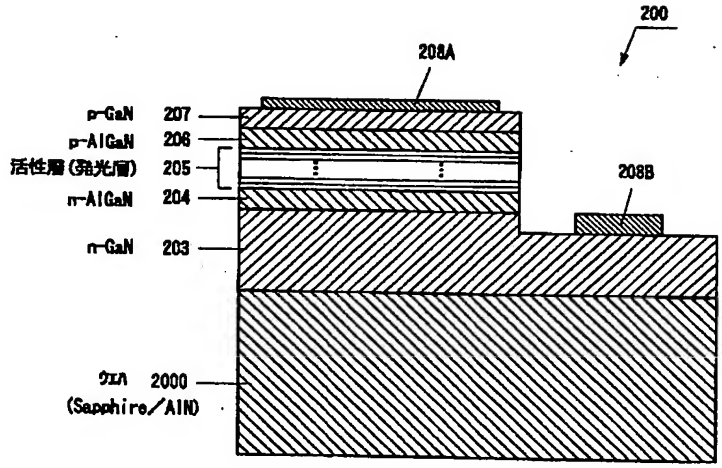
100
109 p-GaN
108 p-AlGaN
107 p-GaN
106 MQW
105 n-GaN
104 n-AlGaN
110B
103 n-GaN
1000
サファイア (Sapphire/AlN)

【図14】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208B
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p-AlGaN 206
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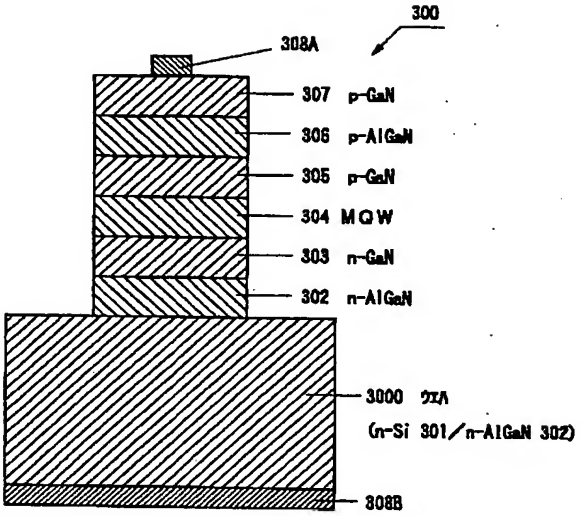
n-GaN 203
サファイア 2000
(Sapphire/AlN)

【図15】



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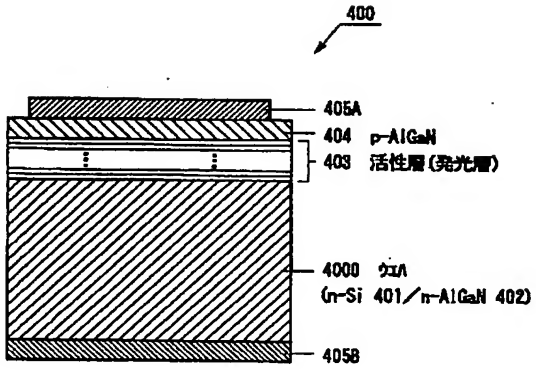

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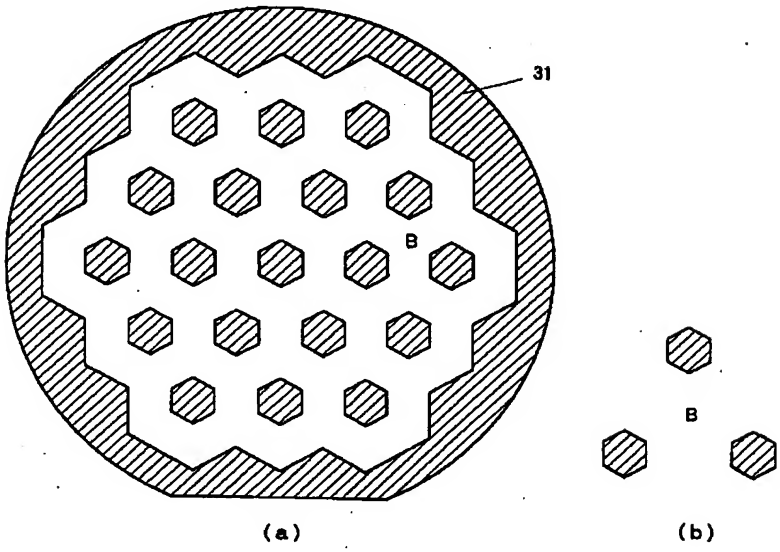

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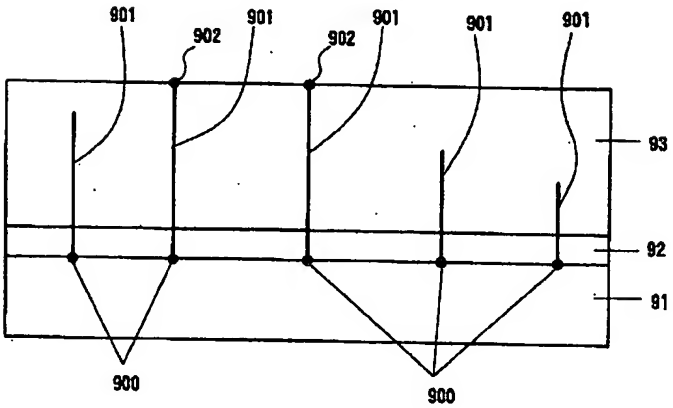

フロントページの続き

Fターム(参考) 5F041 AA03 AA40 AA44 CA04 CA05
CA33 CA34 CA40 CA46 CA65
CA75
5F045 AA03 AA04 AA05 AB09 AB14
AB17 AB18 AC07 AC08 AC12
AF02 AF04 AF09 AF12 BB12
DA53 HA02
5F073 AA45 AA74 CA07 CB04 CB05
CB07 DA05 DA07 DA25 DA35
EA29

Bibliography.

(19) [Country of Issue] Japan Patent Office (JP)
(12) [Official Gazette Type] Open patent official report (A)
(11) [Publication No.] JP,2001-267242,A (P2001-267242A)
(43) [Date of Publication] September 28, Heisei 13 (2001. 9.28)
(54) [Title of the Invention] An III group nitride system compound semiconductor and its manufacture method.
(51) [The 7th edition of International Patent Classification]
H01L 21/205
33/00
H01S 5/343
[FI]
H01L 21/205
33/00 C
H01S 5/343
[Request for Examination] Un-asking.
[The number of claims] 13.
[Mode of Application] OL
[Number of Pages] 18.
(21) [Filing Number] Application for patent 2000-71350 (P2000-71350)
(22) [Filing Date] March 14, Heisei 12 (2000. 3.14)
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[Theme code (reference)]
5F041.
5F045.
5F073.
[F term (reference)]
5F041 AA03 AA40 AA44 CA04 CA05 CA33 CA34 CA40 CA46 CA65 CA75.
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5F073 AA45 AA74 CA07 CB04 CB05 CB07 DA05 DA07 DA25 DA35 EA29.

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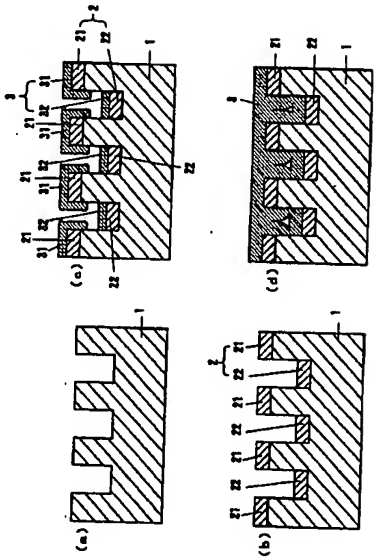

[Translation done.]

* NOTICES *

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1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The manufacture method of the III group nitride system compound semiconductor which

grows up an III group nitride system compound semiconductor on a substrate characterized by providing the following. The process which deletes a part of aforementioned substrate front face [at least], and prepares a level difference in the aforementioned substrate side. They are the method of a wrap, length, and the process that carries out longitudinal direction epitaxial growth also about the lower-berth upper part of the level difference of the aforementioned substrate in a desired III group nitride system compound semiconductor, using as a nucleus the upper surface formed in the front face on which the aforementioned substrate was not deleted at island states, such as the shape of punctiform, the shape of a stripe, and a grid.

[Claim 2] The manufacture method of the III group nitride system compound semiconductor which grows up an III group nitride system compound semiconductor through a buffer layer on a substrate characterized by providing the following. The process which deletes a part of aforementioned substrate front face [at least], and prepares a level difference in the aforementioned substrate side. The process which forms the aforementioned buffer layer in the aforementioned substrate. They are the method of a wrap, length, and the process that carries out longitudinal direction epitaxial growth also about the lower-berth upper part of the level difference of the aforementioned substrate in a desired III group nitride system compound semiconductor, using as a nucleus the aforementioned buffer layer formed in the front face on which the aforementioned substrate was not deleted at island states, such as the shape of punctiform, the shape of a stripe, and a grid.

[Claim 3] The manufacture method of the III group nitride system compound semiconductor which grows up an III group nitride system compound semiconductor through a buffer layer on a substrate characterized by providing the following. The process which deletes a part of aforementioned substrate front face [at least], and prepares a level difference in the aforementioned substrate side. The process which forms the aforementioned buffer layer in the aforementioned substrate. The process which is made to carry out lengthwise epitaxial growth of the III group nitride system compound semiconductor, and forms a single crystal layer on the aforementioned buffer layer. They are the method of a wrap, length, and the process that carries out longitudinal direction epitaxial growth also about the lower-berth upper part of the level difference of the aforementioned substrate in a desired III group nitride system compound semiconductor, using as a nucleus the single crystal layer of the aforementioned III group nitride system compound semiconductor on the aforementioned buffer layer formed in the front face on which the aforementioned substrate was not deleted at island states, such as the shape of punctiform, the shape of a stripe, and a grid.

[Claim 4] The manufacture method of the III group nitride system compound semiconductor which grows up an III group nitride system compound semiconductor through a buffer layer on a substrate characterized by providing the following. The process which forms the aforementioned buffer layer in the aforementioned substrate. The upper case where a part of aforementioned buffer layer and aforementioned substrate front face [at least] were deleted, and the aforementioned buffer layer was formed in the aforementioned substrate side. The process which prepares a level difference with the lower berth in which the aforementioned buffer layer is not formed. They are the method of a wrap, length, and the process that carries out longitudinal direction epitaxial growth also about the lower-berth upper part of the level difference of the aforementioned substrate in a desired III group nitride system compound semiconductor, using as a nucleus the aforementioned buffer layer formed in the front face on which the aforementioned substrate was not deleted at island states, such as the shape of punctiform, the shape of a stripe, and a grid.

[Claim 5] The manufacture method of the III group nitride system compound semiconductor which grows up an III group nitride system compound semiconductor through a buffer layer on a substrate characterized by providing the following. The process which forms the aforementioned buffer layer in the aforementioned substrate. The process which is made to carry out lengthwise epitaxial growth of the III group nitride system compound semiconductor, and forms a single crystal layer on the aforementioned buffer layer. The upper case where a part of single crystal layer of the aforementioned III group nitride system compound semiconductor, aforementioned buffer layer, and aforementioned substrate front face [at least] were deleted, and the single crystal layer of the aforementioned III group nitride system compound semiconductor and the aforementioned buffer layer were formed in the aforementioned substrate side. The process which prepares a level difference with the lower berth in which the single crystal layer of the aforementioned III group nitride system compound semiconductor and the aforementioned buffer layer are not formed, The single crystal layer of the aforementioned III group nitride system compound semiconductor on the aforementioned buffer layer formed in the front face on which the aforementioned substrate was not deleted at island states, such as the shape of punctiform, the shape of a stripe, and a grid, is used as a nucleus. In a desired III group nitride system compound semiconductor, they are the method of a wrap, length, and the process that carries out longitudinal direction epitaxial growth also about the lower-berth upper part of the level difference of the aforementioned substrate.

[Claim 6] The manufacture method of the III group nitride system compound semiconductor which grows up an III group nitride system compound semiconductor on a substrate characterized by providing the following. It is the surface treatment process which forms in the aforementioned substrate front face the portion in which a part of [at least] smoothness on the aforementioned front face of a substrate is worsened, and the aforementioned III group nitride system compound semiconductor layer is not fully formed. The portion in which the aforementioned III group nitride system compound semiconductor was formed in the aforementioned substrate, and the single crystal layer of the aforementioned III group nitride system compound semiconductor was fully formed. It is the process in which the single crystal layer of the aforementioned III group nitride system compound semiconductor forms the portion which is not fully formed. They are the method of a wrap, length, and the process that carries out longitudinal direction epitaxial growth also about the portion by which the single crystal layer of the aforementioned III group nitride system compound semiconductor is not fully formed in the portion which is not worsening the smoothness of the aforementioned substrate in the aforementioned III group nitride system compound semiconductor by using as a nucleus the single crystal layer of the aforementioned III group nitride system compound semiconductor formed in island states, such as the shape of punctiform, the shape of a stripe, and a grid.

[Claim 7] The manufacture method of the III group nitride system compound semiconductor which grows up an III group nitride system compound semiconductor through a buffer layer on a substrate characterized by providing the following. It is the surface treatment process which forms in the aforementioned substrate front face the portion in which a part of [at least] smoothness on the aforementioned front face of a substrate is worsened, and the aforementioned buffer layer is not fully formed. The portion in which the aforementioned buffer layer was formed in the aforementioned substrate, and the aforementioned buffer layer was fully formed. It is the process in which the aforementioned buffer layer forms the portion which is not fully formed. They are the method of a wrap, length, and the process that carries out longitudinal direction epitaxial growth also about the portion by which the aforementioned buffer layer is not fully formed in the portion which is not worsening the smoothness of the aforementioned substrate in the desired III group nitride system compound semiconductor by using as a nucleus the aforementioned buffer layer formed in island states, such as the shape of punctiform, the shape of a stripe, and a grid.

[Claim 8] The manufacture method of the III group nitride system compound semiconductor which grows up an III group nitride system compound semiconductor through a buffer layer on a substrate characterized by providing the following. It is the surface treatment process which forms in the

aforementioned substrate front face the portion in which a part of [at least] smoothness on the aforementioned front face of a substrate is worsened, and the aforementioned buffer layer is not fully formed. The portion in which the aforementioned buffer layer was formed in the aforementioned substrate, and the aforementioned buffer layer was fully formed. It is the process in which the aforementioned buffer layer forms the portion which is not fully formed. The process at which the aforementioned buffer layer forms the single crystal layer of an III group nitride system compound semiconductor in the fully formed portion, The single crystal layer of the aforementioned III group nitride system compound semiconductor on the aforementioned buffer layer of island states, such as the shape of the shape of punctiform and a stripe formed in the portion which is not worsening the smoothness of the aforementioned substrate, or a grid, is used as a nucleus. They are the method of a wrap, length, and the process that carries out longitudinal direction epitaxial growth also about the portion in which the aforementioned buffer layer is not fully formed in the desired III group nitride system compound semiconductor.

[Claim 9] The manufacture method of the III group nitride system compound semiconductor which grows up an III group nitride system compound semiconductor through a buffer layer on a substrate characterized by providing the following. The process which forms the aforementioned buffer layer in the aforementioned substrate. It is the surface treatment process which forms the portion in which a part of [at least] smoothness on the aforementioned front face of a buffer layer is worsened, and the single crystal layer of an III group nitride system compound semiconductor is not fully formed. They are the method of a wrap, length, and the process that carries out longitudinal direction epitaxial growth also about the portion as for which the desired III group nitride system compound semiconductor worsened the smoothness of the aforementioned buffer layer by using as a nucleus the aforementioned buffer layer of island states of the portion which is not worsening the aforementioned smoothness, such as the shape of punctiform, the shape of a stripe, and a grid.

[Claim 10] The manufacture method of the III group nitride system compound semiconductor which grows up an III group nitride system compound semiconductor through a buffer layer on a substrate characterized by providing the following. The process which forms the aforementioned buffer layer in the aforementioned substrate. The process which forms the 1st III group nitride system compound semiconductor on the aforementioned buffer layer. It is the surface treatment process which forms the portion in which a part of [at least] smoothness of the III group nitride system compound semiconductor front face of the above 1st is worsened, and the single crystal layer of the 2nd III group nitride system compound semiconductor is not fully formed. They are the method of a wrap, length, and the process that carries out longitudinal direction epitaxial growth also about the portion as for which the III group nitride system compound semiconductor of the above 2nd worsened the smoothness of the aforementioned buffer layer by using as a nucleus the III group nitride system compound semiconductor of the above 1st of island states of the portion into which the aforementioned smoothness is not getting worse, such as the shape of punctiform, the shape of a stripe, and a grid.

[Claim 11] III group nitride system compound semiconductor element characterized by being formed in the upper layer of the portion in which the aforementioned III group nitride system compound semiconductor layer manufactured by the manufacture method of the III group nitride system compound semiconductor a publication in any 1 term of a claim 1 or a claim 10 carried out longitudinal direction epitaxial growth.

[Claim 12] The III group nitride system compound semiconductor light emitting device characterized by being obtained by carrying out the laminating of the different III group nitride system compound semiconductor layer to the upper layer of the portion in which the aforementioned III group nitride system compound semiconductor layer manufactured by the manufacture method of the III group nitride system compound semiconductor a publication in any 1 term of a claim 1 or a claim 10 carried out longitudinal direction epitaxial growth.

[Claim 13] the manufacture method of an III group nitride system compound semiconductor given in any 1 term of a claim 1 or a claim 10 — in addition, except for the upper layer of the portion which carried out longitudinal direction epitaxial growth — abbreviation — the manufacture method of the III group nitride system compound semiconductor substrate characterized by obtaining the aforementioned III group nitride system compound semiconductor substrate by all removing

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[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] this invention relates to the manufacture method of an III group nitride system compound semiconductor. Especially, it is related with the manufacture method of an III group nitride system compound semiconductor, the III group nitride system compound semiconductor element, and the III group nitride system compound semiconductor substrate using longitudinal direction epitaxial growth (ELO) growth. With an III group nitride system compound semiconductor, in addition, for example, a 2 yuan system like AlN, GaN, and InN, A 3 yuan system like AlxGa1−xN, AlxIn1−xN, and GaxIn1−xN (also any 0< x<1), There are some which are expressed with general formula AlxGayIn1−x−yN (0<=x<=1, 0<=y<=1, 0 <=x+y<=1) which included the 4 yuan system of AlxGayIn1−x−yN (0< x<1, 0< y<1, 0<x+y<1). In addition, especially in this specification, unless it refuses, when only calling it an III group nitride system compound semiconductor, it considers as expression also containing the III group nitride system compound semiconductor by which the impurity for using a conduction type as p type or n type was doped.

[0002]

[Description of the Prior Art] An emission spectrum is a transited [directly] type semiconductor over the large area of ultraviolet shell red, and the III group nitride system compound semiconductor is applied to light emitting devices, such as light emitting diode (Light Emitting Diode) and a laser diode (LD), when it considers as a light emitting device. Moreover, since the band gap can expect operation stabilized in the elevated temperature rather than the element using other semiconductors for a latus reason, the application to transistors, such as FET, is also developed briskly. Moreover, development of various general semiconductor devices also from an environmental side is expected by having not made the arsenic (As) into a principal component. In this III group nitride system compound semiconductor, it usually forms on it, using sapphire as a substrate.

[0003]

[Problem(s) to be Solved by the Invention] However, when an III group nitride system compound semiconductor is formed on silicon on sapphire, transposition occurs by the misfit of the lattice constant of sapphire and an III group nitride system compound semiconductor, and, for this reason, there is a problem that an element property is not good. The transposition by this misfit is penetration transposition which penetrates a semiconductor layer to lengthwise (it is perpendicularly to a substrate side), and has the problem that about [109cm −] two transposition will spread in an III group nitride system compound semiconductor. This spreads III group nitride system compound semiconductor each class from which composition differs to the best layer. Thereby, in the case of a light emitting device, there was a problem that element properties, such as a threshold current of LD and an element life of LD and Light Emitting Diode, did not become good, for example. Moreover, since electrons were scattered about according to the defect also as other semiconductor devices, it remained for becoming the low semiconductor device of mobility (mobility). These were the same when using other substrates..

[0004] The ** type view of drawing 18 explains this. Drawing 18 shows a substrate 91, the buffer layer 92 formed on it, and the III group nitride system compound semiconductor layer 93 further formed on it. As a substrate 91, alumimium nitride (AlN) etc. is conventionally used as buffer layers 92, such as sapphire. Although the buffer layer 92 of alumimium nitride (AlN) is formed the making the misfit of silicon on sapphire 91 and the III group nitride system compound semiconductor layer 93 ease purpose, it still cannot set generating of transposition to 0. From this point 900 generating [transposition], the penetration transposition 901 spreads to lengthwise (it is perpendicularly to a substrate side), and it pierces also through the buffer layer 92 and the III group nitride system compound semiconductor layer 93. In this way, when the laminating of desired various III group nitride system compound semiconductors tends to be carried out to the upper layer of the III group nitride system compound semiconductor layer 93 and it is going to form a semiconductor device in it, penetration transposition will spread the semiconductor device to lengthwise further from,the transposition 902 which arrived at the front face of the III group nitride system compound semiconductor layer 93. Thus, in a Prior art, when forming an III group nitride system compound semiconductor layer, there was a problem that propagation of transposition could not be prevented.

[0005] Made in order that this invention may solve the above-mentioned technical problem, the purpose is manufacturing the III group nitride system compound semiconductor which suppressed generating of penetration transposition.

[0006]

[Means for Solving the Problem] In order to solve the above-mentioned technical problem, invention according to claim 1 In the manufacture method of the III group nitride system compound semiconductor which grows up an III group nitride system compound semiconductor on a substrate Delete a part of substrate front face [at least], and the process which prepares a level difference in a substrate side, and the upper surface formed in the front face on which a substrate was not deleted at island states, such as the shape of punctiform, the shape of a stripe, and a grid, are used as a nucleus. It is characterized by having [a desired III group nitride system compound semiconductor] the method of a wrap, length, and the process that carries out longitudinal direction epitaxial growth also for the lower-berth upper part of the level difference of a substrate.

[0007] Moreover, invention according to claim 2 is set to the manufacture method of the III group nitride system compound semiconductor which grows up an III group nitride system compound semiconductor through a buffer layer on a substrate. The process which deletes a part of substrate front face [at least], and prepares a level difference in a substrate side, and the process which forms a buffer layer in a substrate, It is characterized by having [a desired III group nitride system compound semiconductor] the method of a wrap, length, and the process that carries out longitudinal direction epitaxial growth also for the lower-berth upper part of the level difference of a substrate by using as a nucleus the buffer layer formed in the front face on which a substrate was not deleted at island states, such as the shape of punctiform, the shape of a stripe, and a grid.

[0008] Moreover, invention according to claim 3 is set to the manufacture method of the III group nitride system compound semiconductor which grows up an III group nitride system compound semiconductor through a buffer layer on a substrate. The process which deletes a part of substrate front face [at least], and prepares a level difference in a substrate side, and the process which forms a buffer layer in a substrate, The process which is made to carry out lengthwise epitaxial growth of the III group nitride system compound semiconductor, and forms a single crystal layer on a buffer layer, The single crystal layer of the III group nitride system compound semiconductor on the buffer layer formed in the front face on which a substrate was not deleted at island states, such as the shape of punctiform, the shape of a stripe, and a grid, is used as a nucleus. It is characterized by having [a desired III group nitride system compound semiconductor] the method of a wrap, length, and the process that carries out longitudinal direction epitaxial growth also for the lower-berth upper part of the level difference of a substrate.

[0009] Moreover, invention according to claim 4 is set to the manufacture method of the III group nitride system compound semiconductor which grows up an III group nitride system compound semiconductor through a buffer layer on a substrate. The process which forms a buffer layer in a substrate, and the upper case where a part of buffer layer and substrate front face [at least] were deleted, and the buffer layer was formed in the substrate side, The buffer layer formed in the process which prepares a level difference with the lower berth in which a buffer layer is not formed, and the front face on which a substrate was not deleted at island states, such as the shape of punctiform, the shape of a stripe, and a grid, is used as a nucleus. It is characterized by having [a desired III group nitride system compound semiconductor] the method of a wrap, length, and the process that carries out longitudinal direction epitaxial growth also for the lower-berth upper part of the level difference of a substrate.

[0010] Moreover, invention according to claim 5 is set to the manufacture method of the III group nitride system compound semiconductor which grows up an III group nitride system compound semiconductor through a buffer layer on a substrate. The process which forms a buffer layer in a substrate, and the process which is made to carry out lengthwise epitaxial growth of the III group nitride system compound semiconductor, and forms a single crystal layer on a buffer layer, The upper case where a part of single crystal layer of an III group nitride system compound semiconductor, buffer layer, and substrate front face [at least] were deleted, and the single crystal layer of an III group nitride system compound semiconductor and the buffer layer were formed in the substrate side, The process which prepares a level difference with the lower berth in which the single crystal layer of an III group nitride system compound semiconductor and a buffer layer are not formed, The single crystal layer of the III group nitride system compound semiconductor on the buffer layer formed in the front face on which a substrate was not deleted at island states, such as the shape of punctiform, the shape of a stripe, and a grid, is used as a nucleus. It is characterized by having [a desired III group nitride system compound semiconductor] the method of a wrap, length, and the process that carries out longitudinal direction epitaxial growth also for the lower-berth upper part of the level difference of a substrate.

[0011] Moreover, invention according to claim 6 is set to the manufacture method of the III group nitride system compound semiconductor which grows up an III group nitride system compound semiconductor on a substrate. The surface treatment process which forms in a substrate front face the portion in which a part of [at least] smoothness on the front face of a substrate is worsened,

and an III group nitride system compound semiconductor layer is not fully formed, The portion in which the III group nitride system compound semiconductor was formed in the substrate, and the single crystal layer of an III group nitride system compound semiconductor was fully formed, The process in which the single crystal layer of an III group nitride system compound semiconductor forms the portion which is not fully formed, The single crystal layer of the III group nitride system compound semiconductor formed in island states, such as the shape of punctiform, the shape of a stripe, and a grid, at the portion which is not worsening the smoothness of a substrate is used as a nucleus. It is characterized by having the method of a wrap, length, and the process that carries out longitudinal direction epitaxial growth also for the portion in which the single crystal layer of an III group nitride system compound semiconductor is not fully formed in the III group nitride system compound semiconductor.

[0012] Moreover, invention according to claim 7 is set to the manufacture method of the III group nitride system compound semiconductor which grows up an III group nitride system compound semiconductor through a buffer layer on a substrate. The surface treatment process which forms in a substrate front face the portion in which a part of [at least] smoothness on the front face of a substrate is worsened, and a buffer layer is not fully formed, The portion in which the buffer layer was formed in the substrate and the buffer layer was fully formed, The buffer layer formed in island states, such as the shape of punctiform, the shape of a stripe, and a grid, at the process in which a buffer layer forms the portion which is not fully formed, and the portion which is not worsening the smoothness of a substrate is used as a nucleus. It is characterized by having the method of a wrap, length, and the process that carries out longitudinal direction epitaxial growth also for the portion in which the buffer layer is not fully formed in the desired III group nitride system compound semiconductor.

[0013] Moreover, invention according to claim 8 is set to the manufacture method of the III group nitride system compound semiconductor which grows up an III group nitride system compound semiconductor through a buffer layer on a substrate. The surface treatment process which forms in a substrate front face the portion in which a part of [at least] smoothness on the front face of a substrate is worsened, and a buffer layer is not fully formed, The portion in which the buffer layer was formed in the substrate and the buffer layer was fully formed, The process in which a buffer layer forms the portion which is not fully formed, and the process at which a buffer layer forms the single crystal layer of an III group nitride system compound semiconductor in the fully formed portion, The single crystal layer of the III group nitride system compound semiconductor on the buffer layer of island states, such as the shape of the shape of punctiform and a stripe formed in the portion which is not worsening the smoothness of a substrate, or a grid, is used as a nucleus. It is characterized by having the method of a wrap, length, and the process that carries out longitudinal direction epitaxial growth also for the portion in which the buffer layer is not fully formed in the desired III group nitride system compound semiconductor.

[0014] Moreover, invention according to claim 9 is set to the manufacture method of the III group nitride system compound semiconductor which grows up an III group nitride system compound semiconductor through a buffer layer on a substrate. The process which forms a buffer layer in a substrate, and the surface treatment process which forms the portion in which a part of [at least] smoothness on the front face of a buffer layer is worsened, and the single crystal layer of an III group nitride system compound semiconductor is not fully formed, The portion as for which the desired III group nitride system compound semiconductor worsened the smoothness of a buffer layer by using as a nucleus the buffer layer of island states of the portion which is not worsening smoothness, such as the shape of punctiform, the shape of a stripe, and a grid, the method of a wrap, It is characterized by having length and the process which carries out longitudinal direction epitaxial growth.

[0015] Moreover, invention according to claim 10 is set to the manufacture method of the III group nitride system compound semiconductor which grows up an III group nitride system compound semiconductor through a buffer layer on a substrate. The process which forms a buffer layer in a substrate, and the process which forms the 1st III group nitride system compound semiconductor on a buffer layer, The surface treatment process which forms the portion in which a part of [at least] smoothness of the 1st III group nitride system compound semiconductor front face is worsened, and the single crystal layer of the 2nd III group nitride system compound semiconductor is not fully formed, The 1st III group nitride system compound semiconductor of island states of the portion which is not worsening smoothness, such as the shape of punctiform, the shape of a stripe, and a grid, is used as a nucleus. It is characterized by for the 2nd III group nitride system compound semiconductor worsening the smoothness of a buffer layer, and having also for a portion the method of a wrap, length, and the process that carries out longitudinal direction epitaxial growth.

[0016] Moreover, invention according to claim 11 is III group nitride system compound semiconductor element characterized by being formed in the upper layer of the portion in which the III group nitride system compound semiconductor layer manufactured by the manufacture method of the III group nitride system compound semiconductor a publication in any 1 term of a claim 1 or a claim 10 carried out longitudinal direction epitaxial growth.

[0017] Moreover, invention according to claim 12 is an III group nitride system compound semiconductor light emitting device characterized by being obtained by carrying out the laminating of the different III group nitride system compound semiconductor layer to the upper layer of the portion in which the III group nitride system compound semiconductor layer manufactured by the manufacture method of the III group nitride system compound semiconductor a publication in any 1 term of a claim 1 or a claim 10 carried out longitudinal direction epitaxial growth.

[0018] moreover, invention according to claim 13 — the manufacture method of an III group nitride system compound semiconductor given in any 1 term of a claim 1 or a claim 10 — in addition, except for the upper layer of the portion which carried out longitudinal direction epitaxial growth — abbreviation — it is characterized by obtaining an III group nitride system compound semiconductor substrate by all removing

[0019]

[Function and Effect(s) of the Invention] The outline of the manufacture method of the III group nitride system compound semiconductor of this invention is explained referring to drawing 1 or drawing 11 .

[0020] [Invention of claims 1, 2, and 3] As shown in (a) of drawing 1 , a substrate 1 is deleted in the island state, such as the shape of the shape of a stripe, and a grid, and a level difference is prepared. Next, a buffer layer 2 is formed. Hereafter, as shown in (b) of drawing 1 , a buffer layer 2 explains the case where it consists of the portion 21 mainly formed in the upper case side of the level difference of a substrate 1, and the portion 22 formed in the lower-berth side of a level difference.

[0021] the buffer layer 2 which consists of a portion 21 formed in the upper case side of a level difference of the substrate 1 which has the level difference of island states, such as the shape of the shape of a stripe, and a grid etc. of drawing 1 as shown in (b), and a portion 22 formed in the lower-berth side of a level difference — a nucleus — carrying out — the III group nitride system compound semiconductor 3 — length — and longitudinal direction epitaxial growth is carried out Then, before the III group nitride system compound semiconductor 32 which grows like drawing 1 (c) from the buffer layer 22 formed in the lower-berth side of a level difference buries a level difference, the III group nitride system compound semiconductor 31 which grows considering the buffer layer 21 formed in the upper case side of a level difference as a nucleus can cover the level difference upper

part. Furthermore, length and the density of penetration dislocation which will be spread to lengthwise since the upper part of the level difference of a substrate is covered by longitudinal direction epitaxial growth as shown in (d) of drawing 1 if longitudinal direction growth is carried out decrease extremely the III group nitride system compound semiconductor 3.

[0022] Rather than the III group nitride system compound semiconductor 32 which grows epitaxially to lengthwise from the buffer layer 22 formed in the base of the lower berth of a level difference at this time grows to the upper case of a level difference If it is earlier to coalesce in the longitudinal direction epitaxial growth side from the upper case side of a level difference where the III group nitride system compound semiconductor 31 which grows epitaxially in a longitudinal direction from the buffer layer 21 formed in the upper case side of a level difference faces each other The penetration transposition spread from the buffer layer 22 formed in the base of a level difference in the III group nitride system compound semiconductor 31 upper part of a portion which buried the level difference is suppressed remarkably, and let it be a very good crystalline region. In this case, it will remain as a cavity, without the growth side of the III group nitride system compound semiconductor 32 which grew as a nucleus coming out of the buffer layer 22 formed in the base of a level difference as shown in (d) of drawing 1 to a front face. Coalesce of the growth side of the III group nitride system compound semiconductor 31 which grew considering the buffer layer 21 formed in the upper case side of the level difference of both sides as a nucleus has produced the upper part, and the penetration transposition spread from a buffer layer 22 will be stopped in this cavity.

[0023] Next, when a buffer layer is hardly formed in the side of the level difference of the substrate 1 of drawing 1 as shown in (b), drawing 2 explains the case where a buffer layer is formed also in the side of the level difference of a substrate 1. Drawing 1 (a) Similarly, a substrate 1 is deleted and a level difference is formed ((a) of drawing 2). the buffer layer 2 formed in the upper case side of a level difference of the substrate 1 which has the level difference of island states, such as the shape of the shape of a stripe, and a grid, the lower-berth side of a level difference, and the side of a level difference as shown in (b) of drawing 2 — a nucleus — carrying out — the III group nitride system compound semiconductor 3 — length — and longitudinal direction epitaxial growth is carried out Then, while the III group nitride system compound semiconductor 3 which carries out lengthwise growth from the buffer layer 2 of the lower-berth side of a level difference and the side buries a level difference like drawing 2 (c), it grows up so that the III group nitride system compound semiconductor 3 which carries out longitudinal direction growth from the buffer layer 2 of the upper case side of a level difference may also cover a level difference. In addition, growth of the direction of a normal of the side of a level difference is referred to as growing up in the direction of "length" from the side of a level difference here. Then, as shown in (d) of drawing 1 , the upper part of the level difference of a substrate is closed by the portion in which the III group nitride system compound semiconductor 3 which carries out lengthwise growth from the buffer layer 2 of the side of a level difference buries a level difference, and the III group nitride system compound semiconductor 3 which carries out longitudinal direction growth from the buffer layer 2 of the upper case side of a level difference. The lengthwise penetration dislocation of the III group nitride system compound semiconductor 3 which carries out lengthwise growth from the buffer layer 2 of the side of a level difference is the direction of a normal of the side of a level difference, and its density of the penetration dislocation spread from a substrate side (an upper case side and base) to lengthwise decreases extremely.

[0024] Rather than the III group nitride system compound semiconductor 3 which grows epitaxially to lengthwise from the buffer layer 2 formed in the base of the lower berth of a level difference at this time grows to the upper case of a level difference If it is earlier to coalesce in the longitudinal direction epitaxial growth side from the upper case side of a level difference where the III group nitride system compound semiconductor 3 which grows epitaxially in a longitudinal direction from the buffer layer 2 formed in the upper case side of a level difference faces each other The penetration dislocation spread from the buffer layer 2 formed in the base of a level difference in the III group nitride system compound semiconductor 3 upper part of a portion which buried the level difference is suppressed remarkably, and let it be a very good crystalline region. In this case, it will remain as a cavity, without the growth side of the III group nitride system compound semiconductor 3 which grew as a nucleus coming out of the buffer layer 2 formed in the base of a level difference as shown in (d) of drawing 2 to a front face. The penetration dislocation which coalesce of the growth side of the III group nitride system compound semiconductor 3 which grew considering the buffer layer 2 formed in the upper case side of the level difference of both sides as a nucleus has produced the upper part, and is spread from a buffer layer 2 is [0025] which will be stopped in this cavity. The above quick longitudinal direction epitaxial growth can be easily realized, when the III group nitride system compound semiconductor layer 31 makes {11-20} side the growth side of the direction of the level difference side. What is necessary is just to maintain the upper part with {11-20} side, even if there are few growth sides under this time, for example, longitudinal direction epitaxial growth. Of course, a longitudinal direction epitaxial growth side is not limited to {11-20} side of an III group nitride system compound semiconductor layer.

[0026] The above mentioned can be applied to a substrate also at the III group nitride system compound semiconductor which grows epitaxially directly, without requiring a buffer layer. This is shown in drawing 3 . It is a wrap ((c) of drawing 3) about a level difference by the longitudinal direction growth which used as the nucleus the III group nitride system compound semiconductor 3 of length and the portion which is made to carry out longitudinal direction growth ((b) of drawing 3), and is formed in the upper case side of a level difference for the III group nitride system compound semiconductor 3 after deleting the substrate 1 and forming a level difference ((a) of drawing 3). Moreover, as shown in drawing 4 , the single crystal layer 3 (the single crystal layer 31 of the upper case of a level difference and single crystal layer 32 of the lower berth of a level difference) of an III group nitride system compound semiconductor can be formed in a buffer layer 2 (the buffer layer 21 of the upper case of a level difference, and buffer layer 22 of the lower berth of a level difference) ((b) of drawing 4), and a level difference can also be covered by longitudinal direction growth which used the single crystal layer 31 of the upper case of a level difference as the

[0027] [Invention of claims 4 and 5] As shown in (a) of drawing 5 , a buffer layer 2 is formed on a substrate 1. Next, as shown in (b) of drawing 5 , a buffer layer 2 and a substrate 1 are deleted and a level difference is prepared. here — (c) of drawing 5 — like — the III group nitride system compound semiconductor 31 — mainly — a buffer layer 2 — a nucleus — carrying out — length — and longitudinal direction epitaxial growth is carried out (c) of drawing 5 shows the case where epitaxial growth of the III group nitride system compound semiconductor 32 takes place also from the base and the side of a level difference in part. Rather than the III group nitride system compound semiconductor 32 which grows epitaxially from the base and the side of the lower berth of a level difference grows to the upper case of a level difference at this time If it is earlier to coalesce in the longitudinal direction epitaxial growth side from the upper case side of a level difference where the III group nitride system compound semiconductor 31 which grows epitaxially in a longitudinal direction from the buffer layer 2 formed in the upper case side of a level difference faces each other The penetration transposition spread from the base of a level difference in the III group nitride system compound semiconductor 31 upper part of a portion which buried the level difference is suppressed remarkably, and let it be a very good crystalline region. In this case, it will remain as a cavity, without the growth side of the III group nitride system compound semiconductor 32 which grew from the base of a level difference as shown in (d) of drawing 5 coming out to a front

face. Coalesce of the growth side of the III group nitride system compound semiconductor 31 which grew considering the buffer layer 2 formed in the upper case side of the level difference of both sides as a nucleus has produced the upper part, and the penetration transposition spread from a buffer layer 2 will be stopped in this cavity.

[0028] The above quick longitudinal direction epitaxial growth can be easily realized, when the III group nitride system compound semiconductor layer 31 makes {11-20} side the growth side of the direction of the level difference side. What is necessary is just to maintain the upper part with {11-20} side, even if there are few growth sides under this time, for example, longitudinal direction epitaxial growth. Of course, a longitudinal direction epitaxial growth side is not limited to {11-20} side of an III group nitride system compound semiconductor layer.

[0029] Moreover, as shown in drawing 6 , a buffer layer 2 and the single crystal layer 31 of an III group nitride system compound semiconductor can be formed ((a) of drawing 6), a level difference can be formed ((b) of drawing 6), and a level difference can also be covered by longitudinal direction growth which used the single crystal layer 31 of the upper case of a level difference as the nucleus ((c) of drawing 6 , (d)).

[0030] [Invention of claims 6, 7, and 8] As shown in (a) of drawing 7 , the portion A it was ruined with etching, ******, etc. is formed in substrate 1 front face, and it is made for the portion which is not ruined to be in island states, such as the shape of the shape of a stripe, and a grid. When a buffer layer 2 is formed here, as compared with the buffer layer 21 formed in the portion which is not ruined, a uniform crystal layer is not made as for the buffer layer 22 formed in the portion A ruined [a front face's] to a surface, and a growth rate is slow ((b) of drawing 7). The buffer layer 22 which a single crystal layer is formed at a quick speed by using as a nucleus the buffer layer 21 formed here in the III group nitride system compound semiconductor 3 at length and the portion which is not mainly ruined when longitudinal direction epitaxial growth was carried out, and is formed in the portion A ruined [a front face's] is also covered by growing up to be a longitudinal direction ((c) of drawing 7). Furthermore, when the length of the III group nitride system compound semiconductor 3 and longitudinal direction epitaxial growth are continued, the III group nitride system compound semiconductor 3 which carried out longitudinal direction epitaxial growth will cover completely the buffer layer 22 formed in the portion A ruined [a front face's] by using as a nucleus the buffer layer 21 formed in the portion which is not mainly ruined. At this time, penetration transposition lengthwise [from the buffer layer 22 formed in the portion A ruined / a front face's] will be spread to the III group nitride system compound semiconductor 3 formed in the upper part of longitudinal direction epitaxial growth.

[0031] As shown in (a) of drawing 8 , the portion A it was ruined with etching, ******, etc. is formed in substrate 1 front face, and it is made for the portion which is not ruined to be in island states, such as the shape of the shape of a stripe, and a grid. When the III group nitride system compound semiconductor 3 which grows epitaxially on a substrate 1 is formed here, as compared with the III group nitride system compound semiconductor layer 31 formed in the portion which is not ruined, a uniform single crystal layer is not made as for the III group nitride system compound semiconductor layer 32 formed in the portion A ruined [a front face's] to a surface, and a growth rate is slow ((b) of drawing 8). The III group nitride system compound semiconductor 31 formed in the portion into which the front face of the upper part [III group nitride system compound semiconductor layer 32] which will be formed in the portion A ruined [a front face's] if epitaxial **** is continued on length and the conditions which carry out longitudinal direction epitaxial growth is not mainly ruined will carry out longitudinal direction epitaxial growth of the III group nitride system compound semiconductor 3, and it will cover completely. At this time, penetration transposition lengthwise [from the III group nitride system compound semiconductor 32 formed in the portion A ruined / a front face's] will be spread to the III group nitride system compound semiconductor 31 formed in the upper part of longitudinal direction epitaxial growth.

[0032] furthermore, lengthwise growth of the III group nitride system compound semiconductor 31 is carried out like drawing 9 not on one step of length of an III group nitride system compound semiconductor 3 like drawing 7 , and longitudinal direction epitaxial growth but on the buffer layer 21 formed in the portion which is not ruined probably — making — a single crystal layer — carrying out — a degree — the single crystal layer of this III group nitride system compound semiconductor 31 — a nucleus — carrying out — the III group nitride system compound semiconductor 32 — length — and longitudinal direction growth can be carried out

[0033] [invention of claims 9 and 10] — like drawing 10 , after forming a buffer layer 2 in a substrate 1 ((a) of drawing 10), a front face is got worse by etching and ****** in the front face — making ((b) of drawing 10) — the III group nitride system compound semiconductor 3 — length — and you may carry out longitudinal direction growth ((c) of drawing 10 , (d)) moreover, like drawing 11 , after forming a buffer layer 2 and the III group nitride system compound semiconductor layer 31 in a substrate 1 ((a) of drawing 11), a front face is got worse by etching and ****** in the front face — making ((b) of drawing 11) — the III group nitride system compound semiconductor 33 — length — and you may carry out longitudinal direction growth ((c) of drawing 11 , (d)) Since an III group nitride system compound semiconductor layer is early formed of the portion into which the front face is not getting worse, all can carry out method growth of a wrap also of the portion into which the front face got worse by carrying out longitudinal direction growth by making it into a nucleus.

[0034] The III group nitride system compound semiconductor which has the field which suppressed the penetration transposition spread to lengthwise by the above methods can be formed.

[0035] It can consider as the semiconductor device which has a layer with large mobility with few defects by forming an element in the upper layer of the portion in which the III group nitride system compound semiconductor layer obtained at the above-mentioned process carried out longitudinal direction epitaxial growth (claim 11).

[0036] It can consider as an element life or the light emitting device by which the threshold of LD has been improved by forming a light emitting device in the upper layer of the portion in which the III group nitride system compound semiconductor layer obtained at the above-mentioned process carried out longitudinal direction epitaxial growth (claim 12).

[0037] Moreover, the crystalline good III group nitride system compound semiconductor remarkable [such as transposition,] and suppressed can be obtained by separating only the upper layer of the portion in which the III group nitride system compound semiconductor layer obtained at the above-mentioned process carried out longitudinal direction epitaxial growth from other layers (claim 13). in addition, "abbreviation — removal" all shows that it is included by this invention though the portion in which penetration transposition remained in part is included triggered by the simplicity on manufacture

[0038]

[Embodiments of the Invention] The outline of each example of the gestalt of implementation of the manufacture method of the III group nitride system compound semiconductor of this invention is shown in drawing 1 or drawing 8 . In drawing 1 , the example which is not formed in the side in which the buffer layer 2 was formed of the dicing of a substrate 1 is shown. The dicing of the substrate 1 is carried out, a level difference is formed ((a) of drawing 1), a buffer layer 2 is formed ((b) of drawing 1), and longitudinal direction epitaxial growth of the III group nitride system compound semiconductor layer 3 is carried out ((c) of drawing 1). Before the width of face and the depth of dicing of drawing 1 use as a nucleus the buffer layer 22 formed in the base of a level difference as mentioned above and the III group nitride system compound semiconductor layer 32 which carries

out lengthwise growth buries a level difference, a method decision of a wrap of length and the III group nitride system compound semiconductor layer 31 which carries out longitudinal direction growth is made in the upper part of a level difference by using as a nucleus the buffer layer 21 formed in the upper case side of a level difference. [of (a)] Although the case where a longitudinal direction epitaxial growth side is for example, [11-20] side is assumed in (c) of drawing 1 , this invention is not limited to a growth side. In this way, so that it may coalesce in the upper part of a portion where the dicing of the longitudinal direction growth was carried out by using as a nucleus the buffer layer 21 formed in the upper case side of a level difference, before the portion dicing was carried out [the portion] by lengthwise growth of the base of a level difference is buried The field where penetration transposition was suppressed is formed in the III group nitride system compound semiconductor 31 of the upper part by which dicing was carried out by setting up a dicing configuration and longitudinal direction epitaxial growth conditions ((d) of drawing 1).

[0039] Drawing 2 shows the case where a buffer layer 2 is formed also in the side of the level difference of a substrate 1. This is the same as that of the case of drawing 1 almost.

[0040] Drawing 5 is the gestalt of the operation which formed the buffer layer 2 in the substrate 1 and which carries out after dicing. Lengthwise growth on the base and the side of a level difference of a substrate 1 which the buffer layer 2 is not formed is a wrap ((c) and (d) of drawing 5) about the level difference in which dicing was carried out by the longitudinal direction growth which used as the nucleus the buffer layer 2 which there was nothing, or was very late and was formed in the upper case side of a level difference. The width of face and the depth of dicing of drawing 2 use as a nucleus the buffer layer 21 formed in the upper case side of a level difference before the III group nitride system compound semiconductor layer 32 which carries out lengthwise growth from the base of a level difference as mentioned above buried the level difference, and a method decision of a wrap of length and the III group nitride system compound semiconductor layer 31 which carries out longitudinal direction growth is made in the upper part of a level difference. [of (a)] Although the case where a longitudinal direction epitaxial growth side is for example, [11-20] side is assumed in (c) of drawing 2 , this invention is not limited to a growth side.

[0041] Drawing 7 is the gestalt of the operation which forms a buffer layer 2, after damaging the front face of a substrate 1. the III group nitride system compound semiconductor 3 which used as the nucleus the buffer layer 21 formed in the portion into which area of the portion A ruined [a front face's] etc. is not made as for a uniform single crystal layer to the surface formed on the rough portion A, and the growth rate of a field is not ruined in the late buffer-layer 22 top — length and longitudinal direction epitaxial growth — carrying out — a wrap — it needs — it is determined

[0042] Drawing 8 is the gestalt of the operation which forms an III group nitride system compound semiconductor directly, after damaging the front face of a substrate 1. the III group nitride system compound semiconductor layer 31 formed in the portion into which area of the portion A ruined [a front face's] etc. is not made as for a uniform single crystal layer to the surface formed on the rough portion A, and the growth rate of a field is not ruined in the late III group nitride system compound semiconductor 32 top — length and longitudinal direction epitaxial growth — carrying out — a wrap — it needs — it is determined

[0043] As a gestalt of implementation of the above-mentioned invention, it can choose from degrees, respectively.

[0044] When forming a laminating for an III group nitride system compound semiconductor one by one on a substrate, a III-V group compound semiconductor like sapphire, silicon (Si), silicon carbide (SiC), a spinel (MgAl 2O4), ZnO, the inorganic-crystal substrate of MgO and others, the Lynn-ized gallium, or a gallium arsenide as a substrate or the III group nitride system compound semiconductor of a gallium nitride (GaN) and others can be used.

[0045] Although an organic-metal vapor growth (MOCVD or MOVPE) is desirable as a method of forming an III group nitride system compound semiconductor layer, a molecular-beam vapor growth (MBE), a halide vapor growth (Halide VPE), a liquid phase grown method (LPE), etc. may be used, and each class may be formed by the respectively different growth method.

[0046] For example, in case an III group nitride system compound semiconductor laminating is carried out on silicon on sapphire, in order to make it form with sufficient crystallinity, it is desirable to form a buffer layer that grid mismatching with silicon on sapphire should be corrected. When using other substrates, it is desirable to prepare a buffer layer. III group nitride system compound semiconductor AlxGayIn1-x-yN (0<=x<=1, 0<=y<=1, 0 <=x+y<=1) made to form at low temperature as a buffer layer — AlxGa1-xN (0<=x<=1) is used more preferably A monolayer is sufficient as this buffer layer, and it is good also as a multiplex layer which is [composition] different. The formation method of a buffer layer may be formed at 380-420-degree C low temperature, and the range of it is 1000-1180 degrees C conversely, and it may be formed by the MOCVD method. Moreover, the buffer layer which consists of AlN by the reactive spatter method can also be formed using DC magnetron-sputtering equipment by making high grade metal aluminum and nitrogen gas into raw material. The buffer layer of general formula AlxGayIn1-x-yN (0<=x<=1, 0<=y<=1, 0 <=x+y<=1, and a composition ratio are arbitrary) can be formed similarly. Furthermore, a vacuum deposition, the ion plating method, the laser ablation method, and the efficient consumer response method can be used. As for the buffer layer by the physical vapor deposition, it is desirable to carry out at 200-600 degrees C. It is 300-500 degrees C still more desirably, and is 350-450 degrees C still more desirably. When physical vapor depositions, such as these sputtering methods, are used, buffer layer thickness has desirable 100-3000A. Still more desirably, 100-500A is desirable and is 100-300A most desirably. Moreover, the III group nitride system compound semiconductor of the III group nitride system compound semiconductor layer used as the nucleus of growth of longitudinal direction epitaxial growth and/or the upper layer makes one period a buffer layer and a single crystal III group nitride system compound semiconductor layer. and is good also as a layer (basal layer) which carried out multiplex period formation. Moreover, when using a basal layer, the best layer has a more desirable single crystal layer as a layer used as the nucleus of longitudinal direction epitaxial growth.

[0047] A buffer layer, the III group nitride system compound semiconductor layer used as the nucleus of growth of longitudinal direction epitaxial growth, The III group nitride system compound semiconductor of the layer which carries out longitudinal direction epitaxial growth, and/or the upper layer Whether it replaces with boron (B) and a thallium (Tl) or a part of composition of an III group element replaces composition of nitrogen (N) part by Lynn (P), the arsenic (As), antimony (Sb), and the bismuth (Bi), it can apply this invention substantially. Moreover, what doped the grade which cannot display these elements on composition may be used. For example, AlxGa1-xN (0<=x<=1) which is the III group nitride system compound semiconductor which does not have an indium (In) and an arsenic (As) in composition may be compensated for the extended distortion of the crystal by the omission of a nitrogen atom with compressive strain with doping the big indium (In) of an atomic radius from aluminum (aluminum) and a gallium (Ga), and doping (As) with a big atomic radius from nitrogen (N), and crystallinity may be improved. In this case, since acceptor impurity goes into the position of an III group atom easily, p type crystal can also be obtained by the AZUGU.loan. Thus, together with the invention in this application, penetration transposition can also be further lowered to 100 or about 1/1000 by improving crystallinity. In addition, when it constitutes as a light emitting device, it is desirable to use the 2 yuan system of an III group nitride system compound semiconductor or a 3 yuan system originally.

[0048] When forming an n type III group nitride system compound semiconductor layer, IV group

elements, such as Si, germanium, Se, Te, and C, or VI group element can be added as an n type impurity. Moreover, as a p type impurity, II group elements, such as Zn, Mg, Be, calcium, Sr, and Ba, or IV group element can be added. You may dope plurality or n type impurity, and p type impurity for these in the same layer.

[0049] Although that from which a growth side becomes perpendicular to a substrate as longitudinal direction epitaxial growth is desirable, you may grow up to a substrate with a slanting facet side.

[0050] As longitudinal direction epitaxial growth, the upper part and a substrate side have the perpendicular more desirable thing of a longitudinal direction epitaxial growth side, and it is more desirable for all to be {11-20} sides of an III group nitride system compound semiconductor further at least.

[0051] In case it **********s, a level difference is prepared from the relation between the depth and width of face so that it may be closed by longitudinal direction epitaxial growth. At this time, the lengthwise growth from a different layer also uses a late thing in an initial stage at least.

[0052] When the crystal orientation of the III group nitride system compound semiconductor layer which carries out a laminating on a substrate can be expected, it is useful to give a mask or dicing in the shape of a stripe so that the level difference side of a substrate may become parallel to the a-th page ({11-20} side) of an III group nitride system compound semiconductor layer or the m-th page ({1-100} side). In addition, you may design the above-mentioned stripe and a mask arbitrarily the shape of an island, in the shape of a grid, etc. The growth side of a slanting angle is sufficient as a longitudinal direction epitaxial growth side to a substrate side besides a thing perpendicular to a substrate side. Suppose that it is perpendicular in the field whose longitudinal direction of a stripe is the m-th page of an III group nitride system compound semiconductor layer for making a field into a longitudinal direction epitaxial growth side (1-100) as a-th page of an III group nitride system compound semiconductor layer (11-20). For example, since the m-th page of sapphire is usually in agreement with the a-th page of the III group nitride system compound semiconductor layer formed on it when [both] making a substrate into the a-th page of sapphire, or the c-th page, dicing is given according to this. When considering as the shape of punctiform and an island of the shape of a grid, and others, it is desirable that it is in agreement with {11-20} side of an III group nitride system compound semiconductor layer in which each field which forms a profile (side attachment wall) is formed up.

[0053] An etching mask can have oxides, such as oxidization silicon (SiO2), a silicon nitride (Si3N4), titanium oxide (TiOX), and a zirconium oxide (ZrOX), nitrides, and these multilayers, and can be. These membrane formation methods are arbitrary besides vapor growths, such as vacuum evaporationo, a spatter, and CVD.

[0054] Although reactant ion beam etching (RIBE) is desirable when etching, the arbitrary etching methods can be used. Moreover, it may replace with etching and a level difference may be formed by the mechanical methods, such as scribing. When damaging a front face, ****** by scribing and the diamond cutter etc. is arbitrary.

[0055] Semiconductor devices, such as FET and a light emitting device, can be formed in the upper part centering on the field where the whole III group nitride system compound semiconductor which has the field where the above-mentioned penetration transposition was suppressed, or penetration transposition was suppressed. In the case of a light emitting device, although a luminous layer can consider the thing of gay structure besides multiplex quantum well structure (MQW) and single quantum well structure (SQW), hetero structure, and double hetero structure, you may form by the pin junction or pn junction.

[0056] The portion by which the penetration transposition which prepared the level difference by the substrate 1, the buffer layer 2, and dicing is not suppressed in the III group nitride system compound semiconductor which has the field where above-mentioned penetration transposition was suppressed can be removed, and it can consider as an III group nitride system compound semiconductor substrate. It can use as a substrate for forming a bigger III group nitride system compound semiconductor crystal possible [forming III group nitride system compound semiconductor element besides]. As the removal method, it is arbitrary besides mechanochemical polishing.

[0057] As application of this invention, after forming a field with little penetration transposition by substrate processing, forming a field with little penetration transposition in the field upper part with much penetration transposition is also further included by this invention using longitudinal direction epitaxial growth. For example, an III group nitride system compound semiconductor layer with little [as a whole] penetration transposition can be obtained by covering the mask upper part by longitudinal direction epitaxial growth by using as a nucleus a field front face with little penetration transposition which forms a mask in the field with much penetration transposition of the III group nitride system compound semiconductor layer which has a field with little penetration transposition, and many fields by the means of the claim 1 of this invention, or a claim 4, and does not form the mask. In addition, the 2nd longitudinal direction epitaxial growth in the field upper part with much penetration transposition is arbitrary.

[0058] Hereafter, it explains based on the concrete example of invention. Although a light emitting device is raised as an example, this invention is not limited to the following example and is indicating the applicable [to arbitrary elements] manufacture method.

[0059] The III group nitride system compound semiconductor of this invention was manufactured by the vapor growth by the organometallic compound vapor growth (it is indicated as "MOVPE" below). The used gas is ammonia (NH3), carrier gas (H2 or N2), trimethylgallium (it is described as "TMG" Ga (CH3)3 and the following), a trimethylaluminum (it is described as "TMA" aluminum (CH3)3 and the following), trimethylindium (it is described as "TMI" In (CH3)3 and the following), and magnesium cyclopentadienyl (it is described as "Cp2Mg" Mg (C5H5)2

[0060] The [1st example] The a-th page washed with organic washing and heat treatment was made into the principal plane, and the level difference of the shape of a stripe with width of face of 10 micrometers, an interval [of 10 micrometers], and a depth of 10 micrometers was formed for the silicon on sapphire 1 of a single crystal by dicing. Next, temperature was made into 400 degrees C, 10 L/min and NH3 were supplied by 5 L/min, TMA was supplied for H2 for about 3 minutes by 20micromol/min, and the buffer layer 2 of AlN was formed in the thickness of about 40nm. The buffer layer 2 was formed in the upper case side and the base at the Lord of the level difference of a substrate 1.

[0061] Next, the temperature of silicon on sapphire 1 was held at 1150 degrees C, 20 L/min and NH3 were introduced by 10 L/min, TMG was introduced for H2 by 5micromol/min, and the GaN layer 3 was formed by length and longitudinal direction epitaxial growth. At this time, the level difference was covered by the longitudinal direction epitaxial growth from the buffer layer 21 mainly formed in the upper case side of a level difference, and the front face became flat ((c) of drawing 1). 20 L/min and NH3 were introduced by 10 L/min, TMG was introduced after this and for H2 by 300micromol/min, the GaN layer 3 was grown up, and it considered as the thickness of 10 micrometers. As compared with the portion by which the portion formed in the base upper part of a level difference with a depth [of the GaN layer 3 / of a substrate 1] of 10 micrometers was formed in the upper case side upper part of a level difference, penetration transposition was stopped remarkably.

[0062] The [2nd example] The a-th page washed with organic washing and heat treatment was made into the principal plane, temperature of the silicon on sapphire 1 of a single crystal was made into

400.degrees C, 10 L/min and NH3 were supplied by 5 L/min, TMA was supplied for H2 for about 3 minutes by 20micromol/min, and the buffer layer 2 of AlN was formed in the thickness of about 40nm. Next, by dicing, the level difference was formed with width of face of 10 micrometers, an interval [of 10 micrometers], and a depth of 10 micrometers in the shape of a stripe. The buffer layer 2 remained only in the upper case side of the level difference of a substrate 1 ((b) of drawing 5).

[0063] Next, the temperature of silicon on sapphire 1 was held at 1150 degrees C, 20 L/min and NH3 were introduced by 10 L/min, TMG was introduced for H2 by 5micromol/min, and the GaN layer 3 was formed by length and longitudinal direction epitaxial growth. At this time, the level difference was covered by the longitudinal direction epitaxial growth from the buffer layer 21 mainly formed in the upper case side of a level difference, and the front face became flat ((c) and (d) of drawing 5). 20 L/min and NH3 were introduced by 10 L/min, TMG was introduced after this and for H2 by 300micromol/min, the GaN layer 3 was grown up, and it considered as the thickness of 10 micrometers. As compared with the portion by which the portion formed in the base upper part of a level difference with a depth [of the GaN layer 3 / of a substrate 1] of 10 micrometers was formed in the upper case side upper part of a level difference, penetration transposition was stopped remarkably.

[0064] The [3rd example] The a-th page washed with organic washing and heat treatment was made into the principal plane, short-time etching of the silicon on sapphire 1 of a single crystal was carried out by the selection dry etching using reactant ion beam etching (RIBE) at the shape of width of face of 10 micrometers, the interval of 10 micrometers, and a stripe, and the field dry area was started. Next, temperature was made into 400 degrees C, 10 L/min and NH3 were supplied by 5 L/min, TMA was supplied for H2 for about 3 minutes by 20micromol/min, and the buffer layer 2 of AlN was formed in the thickness of about 40nm. Surface morphology differed in the portion 22 whose buffer layers 2 are not the portion 22 of a field dry area, and a field dry area ((b) of drawing 7).

[0065] Next, the temperature of silicon on sapphire 1 was held at 1150 degrees C, 20 L/min and NH3 were introduced by 10 L/min, TMG was introduced for H2 by 5micromol/min, and the GaN layer 3 was formed by length and longitudinal direction epitaxial growth. The portion of a field dry area was covered by the longitudinal direction epitaxial growth from the portion 21 which is not mainly a field dry area at this time, and the front face became flat ((c) and (d) of drawing 7). 20 L/min and NH3 were introduced by 10 L/min, TMG was introduced for this ** and H2 by 300micromol/min, the GaN layer 3 was grown up, and it considered as the thickness of 3 micrometers. As compared with the portion by which the portion formed in the base upper part of a level difference with a depth [of the GaN layer 3 / of a substrate 1] of 10 micrometers was formed in the upper case side upper part of a level difference, penetration transposition was stopped remarkably.

[0066] The [4th example] In this example, the layer (basal layer) which carried out multiplex period formation was used by making a buffer layer like drawing 12 , and a single crystal III group nitride system compound semiconductor layer into one period. Temperature was reduced to 400 degrees C on the silicon on sapphire 1 of a single crystal by making into a principal plane the a-th page washed with organic washing and heat treatment, 10 L/min and NH3 were supplied by 5 L/min, TMA was supplied for H2 for about 3 minutes by 20micromol/min, and the 1st AlN layer 211 was formed in the thickness of about 40nm. Next, the temperature of silicon on sapphire 1 was held at 1000 degrees C, 20 L/min and NH3 were introduced by 10 L/min, TMG was introduced for H2 by 300micromol/min, and the GaN layer 212 of about 0.3 micrometers of thickness was formed. Next, temperature was reduced to 400 degrees C, 10 L/min and NH3 were supplied by 5 L/min, TMA was supplied for H2 for about 3 minutes by 20micromol/min, and the 2nd AlN layer 213.was formed in the thickness of about 40nm. In this way, the basal layer 20 which consists of the 1st AlN layer 211 of about 40nm of thickness, the GaN layer 212 of about 0.3 micrometers of thickness, and the 2nd AlN layer 213 of about 40nm of thickness was formed.

[0067] Next, the level difference was formed by dicing like the 2nd example. The dicing depth of silicon on sapphire 1 was set to 10 micrometers. Next, the temperature of silicon on sapphire 1 was held at 1150 degrees C, 20 L/min and NH3 were introduced by 10 L/min, TMG was introduced for H2 by 5micromol/min, and the GaN layer 3 was formed by longitudinal direction epitaxial growth. In this way, the level difference was covered by longitudinal direction epitaxial growth by having used as the nucleus the basal layer 20 mainly formed in the upper case side of a level difference, and the front face became flat. 20 L/min and NH3 were introduced by 10 L/min, TMG was introduced after this and for H2 by 300micromol/min, the GaN layer 3 was grown up, and the GaN layer 3 was made into the thickness of 10 micrometers. As compared with the portion by which the portion formed in the base upper part of a level difference with a depth [of the GaN layer 3 / of silicon on sapphire 1] of 10 micrometers was formed in the upper case side upper part of a level difference, penetration transposition was stopped remarkably.

[0068] The [5th example] A laser diode (LD) 100 like drawing 13 was formed as follows on the wafer formed like the 1st example. However, at the time of formation of the GaN layer 3, the silane (SiH4) was introduced and the GaN layer 3 was used as the layer which consists of n type GaN of a silicon (Si) dope. In addition, in order to make drawing simple, the GaN layer 3 of the portion which is burying the buffer layer 2 and level difference which were formed in the upper case side and base of the silicon on sapphire 1 which has a level difference, and a level difference is combined, it is indicated as a wafer 1000, and the other GaN layer 3 is indicated to be the GaN layer 103.

[0069] The silicon on sapphire which has a level difference, the buffer layer which consists of AlN, and its level difference in the wafer layer 1000 and the n type GaN layer 103 which consist of a wrap n type GaN layer Silicon (Si) n clad layer 104 which consists of aluminum0.08Ga0.92N of a dope, n guide layer 105 which consists of GaN of a silicon (Si) dope, the luminous layer 106 of MQW structure, p guide layer 107 which consists of GaN of a magnesium (Mg) dope, magnesium (Mg) p clad layer 108 which consists of aluminum0.08Ga0.92N of a dope, and p contact layer 109 which consists of GaN of a magnesium (Mg) dope were formed. Next, electrode 110B which **********s in part and consists of aluminum (aluminum) was formed until a total of three steps of GaN layers 103 of two steps of GaN layers and n type GaN layers exposed electrode 110A which consists of gold (Au) on p contact layer 109. Thus, an element life and luminous efficiency of the laser diode (LD) formed improved remarkably.

[0070] The [6th example] Light emitting diode (Light Emitting Diode) 200 like drawing 14 was formed as follows on the wafer formed like the 1st example. However, at the time of formation of the GaN layer 3, the silane (SiH4) was introduced and the GaN layer 3 was used as the layer which consists of n type GaN of a silicon (Si) dope. In addition, in order to make drawing simple, the GaN layer 3 of the portion which is burying the buffer layer 2 and level difference which were formed in the upper case side and base of the silicon on sapphire 1 which has a level difference, and a level difference is combined, it is indicated as a wafer 2000, and the other GaN layer 3 is indicated to be the GaN layer 203.

[0071] n clad layer 204 which consists of aluminum0.08Ga0.92N of a silicon (Si) dope, the luminous layer 205, p clad layer 206 which consists of aluminum0.08Ga0.92N of a magnesium (Mg) dope, and p contact layer 207 which consists of GaN of a magnesium (Mg) dope were formed on the wafer 2000 which consists of silicon on sapphire, the buffer layer which consists of AlN, and the GaN layer which buries a level difference, and the n type GaN layer 203. Next, electrode 208B which

**********s in part and consists of aluminum (aluminum) was formed until two steps of GaN layers, a GaN layer and an n type GaN layer, 203 exposed electrode 208A which consists of gold (Au) on p contact layer 207. Thus, an element life and luminous efficiency of light emitting diode (Light Emitting Diode) formed improved remarkably.

[0072] The [7th example] In this example, the silicon (Si) substrate was used as a substrate. The silicon (Si) substrate 301 was **********ed by etching with width of face of 10 micrometers, an interval [of 10 micrometers], and a depth of 10 micrometers in the shape of a stripe. next, the ** silane (SiH4) which held the temperature of a silicon substrate 301 at 1150 degrees C, and 10 L/min and TMG were diluted by 5micromol/min, and was diluted [2 / H/ 3 / NH/ 20 L/min and] by 0.5micromol/min and H2 gas in TMA — 0.01micromol/min — supplying — the upper case side of the level difference of a silicon substrate, the side, and a base to n-aluminum0.15Ga0.85N layer — length — and longitudinal direction growth was carried out In this way, the ** silane (SiH4) which 10 L/min and TMG were diluted by 100micromol/min, and was diluted [2 / H/ after level difference is covered by the longitudinal direction epitaxial growth which mainly uses upper case side as nucleus and front face becomes flat / 3 / NH/ 10 L/min and] by 10micromol/min and H2 gas in TMA was supplied by 0.2micromol/min, the n-aluminum0.15Ga0.85N layer was grown up, and it considered as the thickness of 3 micrometers. Hereafter, n-aluminum0.15Ga0.85N layer 302 is combined with a silicon substrate 301, and it is indicated as a wafer 3000.

[0073] n guide layer 303 which consists of GaN of a silicon (Si) dope, the luminous layer 304 of MQW structure, p guide layer 305 which consists of GaN of a magnesium (Mg) dope, p clad layer 306 which consists of aluminum0.08Ga0.92N of a magnesium (Mg) dope, and p contact layer 307 which consists of GaN of a magnesium (Mg) dope were formed as mentioned above on the wafer 3000 (the silicon substrate 301 which has a level difference, and n-aluminum0.15Ga0.85N layer 302 which Next, electrode 308B which changes electrode 308A which consists of gold (Au) on p contact layer 307 from aluminum (aluminum) to silicon-substrate 301 rear face was formed. Thus, an element life and luminous efficiency of the laser diode (LD) 300 of formed drawing 15 improved remarkably.

[0074] [Octavus example] this example also used the silicon (Si) substrate as a substrate. Like n-aluminum0.15Ga0.85N layer 302 formed in the silicon substrate 301 which has the level difference of the 7th example, the silicon substrate 401 which has a level difference, and the wafer 4000 of n-aluminum0.15Ga0.85N layer 402 formed on it were prepared, and the luminous layer 403 and p clad layer 404 which consists of aluminum0.15Ga0.85N of a magnesium (Mg) dope were formed. Next, electrode 405B which changes electrode 405A which consists of gold (Au) on p clad layer 404 from aluminum (aluminum) to silicon-substrate 401 rear face was formed. Thus, an element life and luminous efficiency of light emitting diode (Light Emitting Diode) 400 of formed drawing 16 improved remarkably.

[0075] [Deformation of etching] Drawing 17 is an example which forms the upper case of a level difference, or the field dry-area portion B and the portion which does not start a field dry area in the shape of an island again. This is the ** type view simplified for the understanding, and (a) of drawing 17 may form 10 million number upper cases of an island-like level difference per wafer in fact, although the periphery is also shown. In (a) of drawing 17 , the base B of a level difference (the field dry-area portion [as opposed to / the portion which does not start a field dry area / Or] B) has one 3 times the area of this to the upper case of an island-like level difference. In (b) of drawing 17 , the base B of a level difference (the field dry-area portion [as opposed to / the portion which does not start a field dry area / Or] B) has one 8 times the area of this to the upper case of an island-like level difference.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The cross section showing the manufacturing process of the III group nitride system compound semiconductor concerning the 1st example of this invention.

[Drawing 2] The cross section showing the manufacturing process of another III group nitride system compound semiconductor of this invention.

[Drawing 3] The cross section showing the manufacturing process of the III group nitride system compound semiconductor concerning the 7th example of this invention.

[Drawing 4] The cross section showing the manufacturing process of another III group nitride system compound semiconductor of this invention.

[Drawing 5] The cross section showing the manufacturing process of the III group nitride system compound semiconductor concerning the 2nd example of this invention.

[Drawing 6] The cross section showing the manufacturing process of another III group nitride system compound semiconductor of this invention.

[Drawing 7] The cross section showing the manufacturing process of the III group nitride system compound semiconductor concerning the 3rd example of this invention.

[Drawing 8] The cross section showing the manufacturing process of another III group nitride system compound semiconductor of this invention.

[Drawing 9] The cross section showing the manufacturing process of still more nearly another III group nitride system compound semiconductor of this invention.

[Drawing 10] The cross section showing the manufacturing process of still more nearly another III group nitride system compound semiconductor of this invention.

[Drawing 11] The cross section showing the manufacturing process of still more nearly another III group nitride system compound semiconductor of this invention.

[Drawing 12] The cross section showing the manufacturing process of the III group nitride system compound semiconductor concerning the 4th example of this invention.

[Drawing 13] The cross section showing the structure of the III group nitride system compound semiconductor light emitting device concerning the 5th example of this invention.

[Drawing 14] The cross section showing the structure of the III group nitride system compound semiconductor light emitting device concerning the 6th example of this invention.

[Drawing 15] The cross section showing the structure of the III group nitride system compound semiconductor light emitting device concerning the 7th example of this invention.

[Drawing 16] The cross section showing the structure of the III group nitride system compound semiconductor light emitting device concerning the example of the octavus of this invention.

[Drawing 17] The ** type view showing other examples of etching of the 1st III group nitride system

compound semiconductor.

[Drawing 18] The cross section showing the penetration transposition which spreads an III group nitride system compound semiconductor.

[Description of Notations]

1,101,201,301,401 Substrate

1000, 2000, 3000, 4000 Wafer which consists the substrate and buffer layer which have a level difference, and a level difference of a wrap III group nitride system compound semiconductor layer

2 Buffer Layer

20 Basal Layer

31, 32, 33 III group nitride system compound semiconductor

103 203 n-GaN layer

104, 204, 302, 402 n-AlGaN clad layer

105 303 n-GaN guide layer

106, 205, 304, 403 Luminous layer

107 305 p-GaN guide layer

108, 206, 306, 404 p-AlGaN clad layer

109, 207, 307 p-GaN layer

110A, 208A, 308A, 405A p electrode

110B, 208B, 308B, 405B n electrode

[Translation done.]

* NOTICES *

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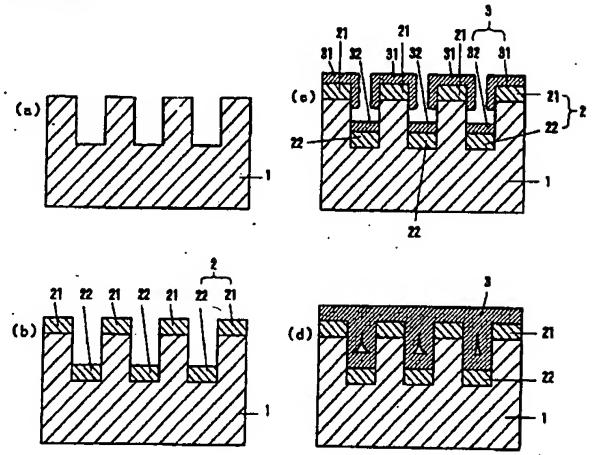
1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

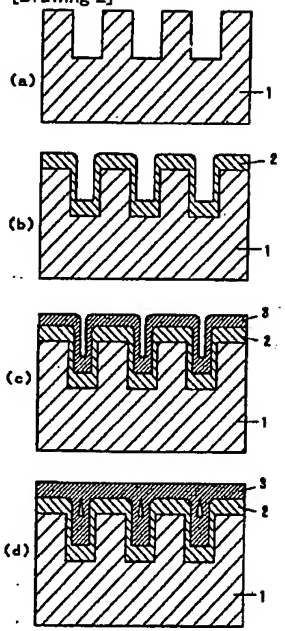
3.In the drawings, any words are not translated.

DRAWINGS

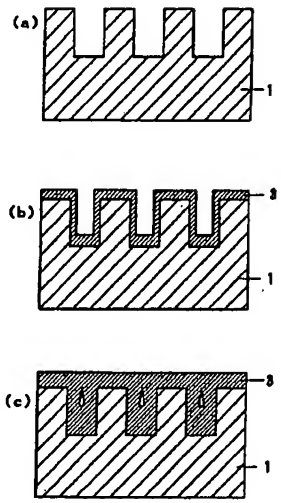
[Drawing 1]



[Drawing 2]



[Drawing 3]



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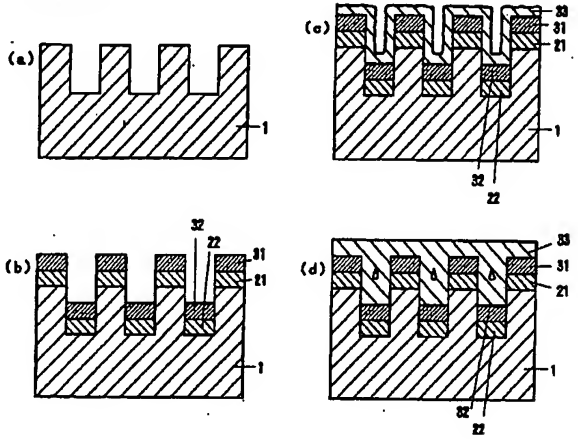

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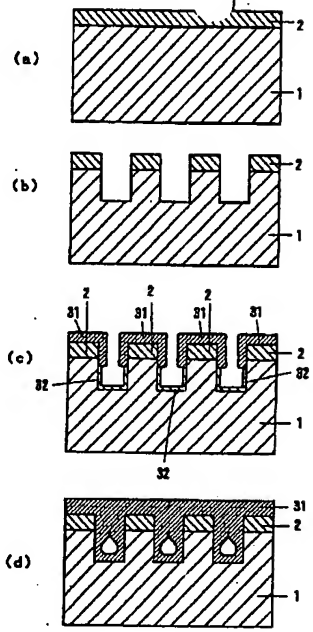

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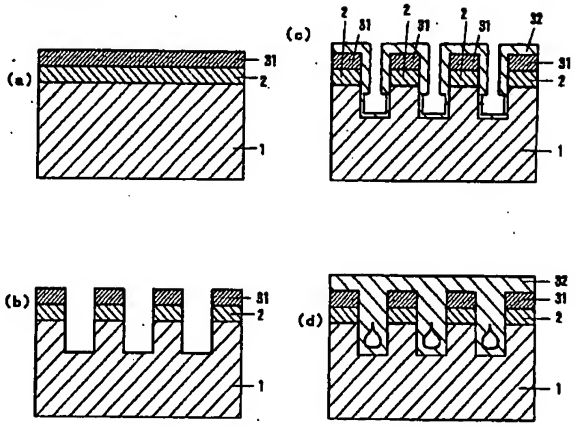

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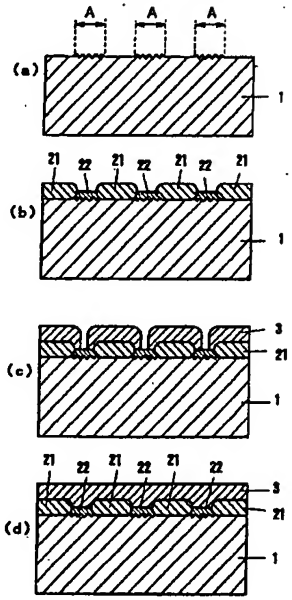

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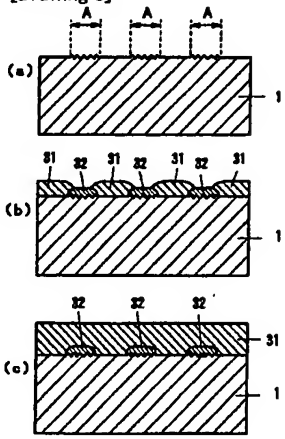

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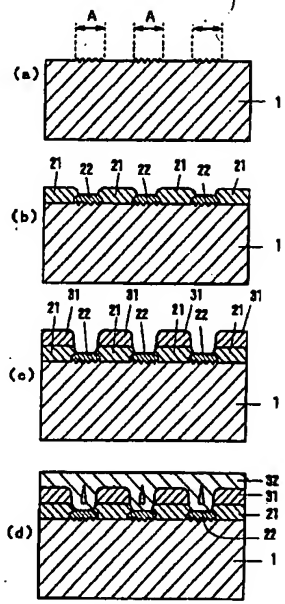

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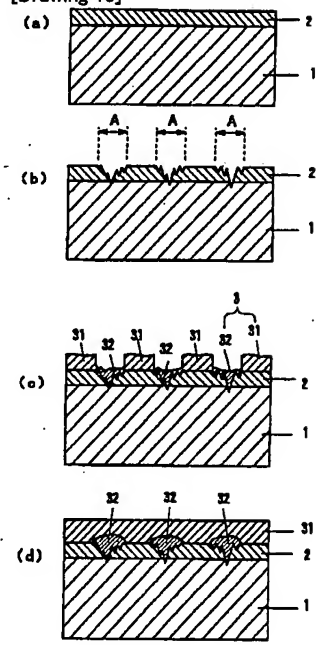

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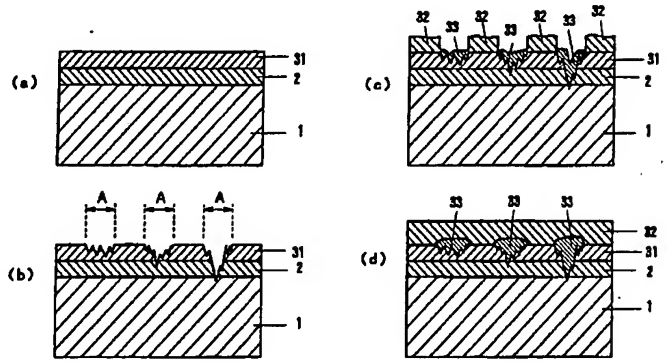

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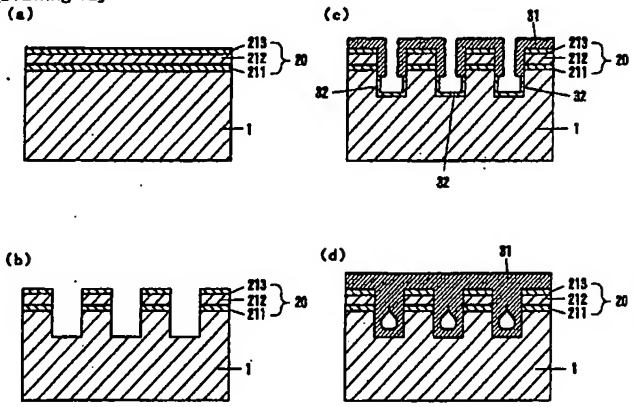

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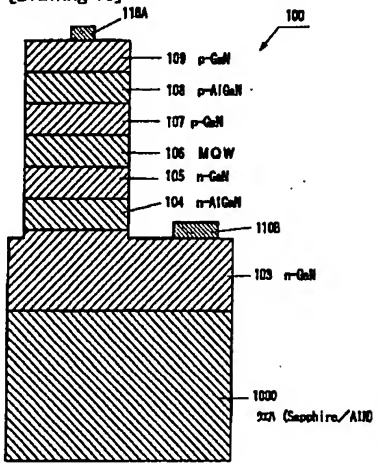

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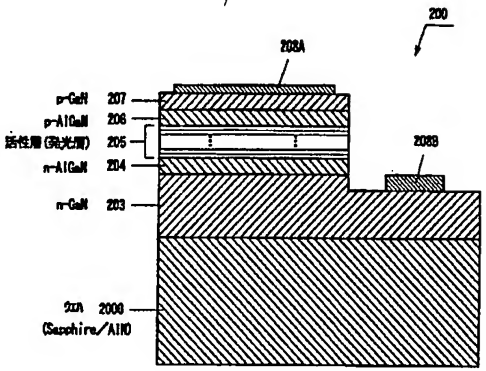

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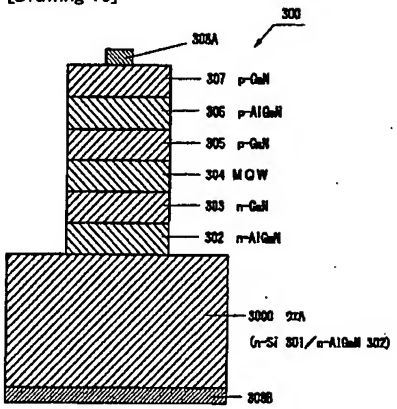

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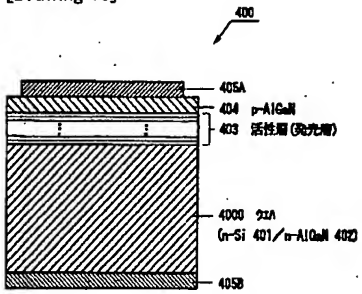
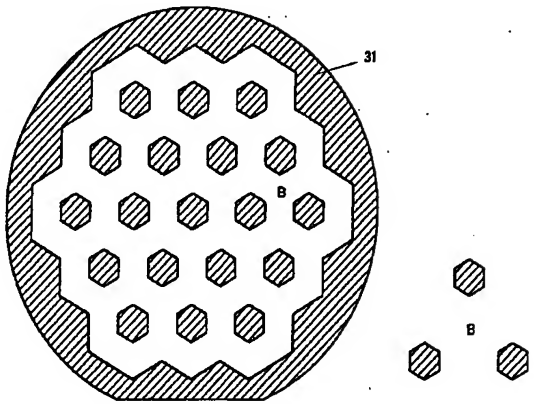


[Drawing 17]



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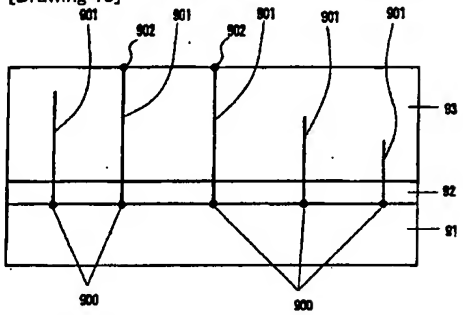

[Translation done.]